



Syrinx-DualVME

Dual Digital FM Demodulator

Technical Manual

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Chapter 1 Introduction

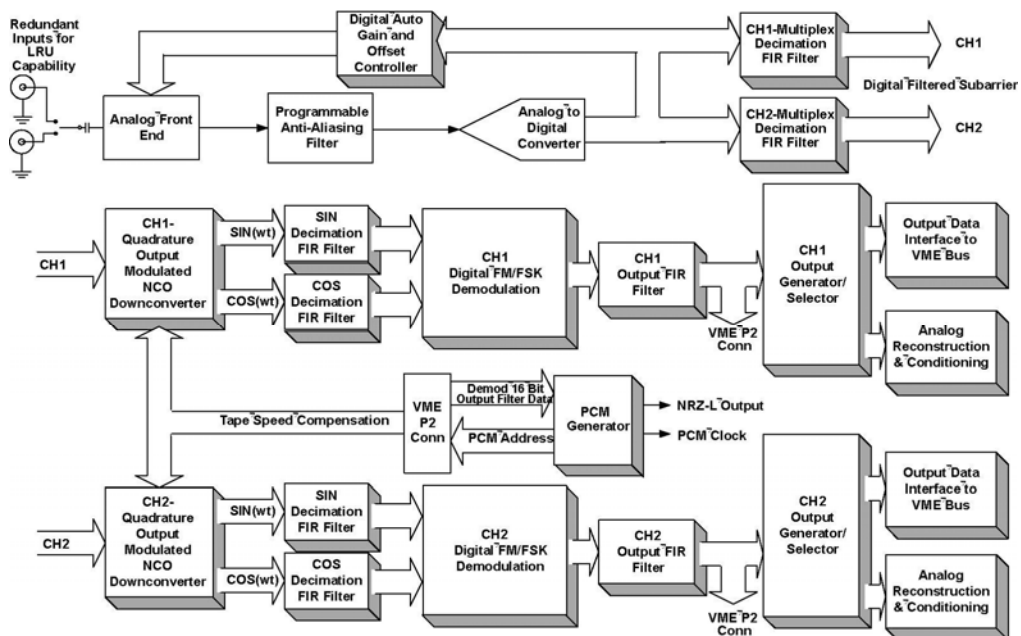
1.1. Overview of Syrinx-DualVME

The Syrinx-DualVME Digital FM Demodulator is a DSP (Digital Signal Processing) based two-channel FM demodulator packaged in a VME 6U form factor. Built In Test (BIT) feature, with the accuracy of an external calibrator, allows the user to verify demod setup and functionality. DSP algorithms are implemented in state-of-the-art FPGAs (Field Programmable Gate Arrays) allowing for rapid enhancements or customization.

With two fully programmable demodulator channels per card, each capable of demodulating FM/FM, FM/PCM, and FSK, the Syrinx-DualVME is the most flexible VME based FM demodulator available. All IRIG 106-93 CBW and PBW FM subcarriers are supported as well as non-standard frequencies with a carrier frequency range of 250 Hz to 3.5 MHz and a digital output filter frequency range of 1 Hz to 1 MHz. Additional recommended applications of the Syrinx-DualVME card include tone detection and pre-detection of antenna AGC signals. The PCM Frame Generator feature allows the user to encode demodulated data from multiple cards into a single NRZ-L or RNRZ-L PCM data stream for digital storage or transmission.

By using DSP based algorithms, including Finite Impulse Response (FIR) filters, multi-stage recursive decimation filters, Modulated Numerically Controlled Oscillators (MNCO) and DSP implemented Phase-Locked Loops (PLL); the Syrinx-DualVME eliminates the need for calibration and tuning. C++ language source code is supplied which aids in creating integrated instrument software for complex VME applications.

The input subcarrier is received in analog form, conditioned with a digital auto gain control circuit, and fed into a sophisticated anti-alias filter prior to a 12-bit digitizer (see block diagram below). The demodulated output is available in both analog and digital formats. The analog data is reconstructed using a programmable reconstruction filter, then normalized to user specified output levels and offsets. The digital data is available through a FIFO circuit for direct storage to the host computer for FFT analysis, or via a PCM stream generated by the on-board PCM Frame Generator.



1.2. Specifications

Input Specifications

| | |
|----------------------------------|--|
| Input Subcarrier Frequency Range | 250 Hz to 3.5 MHz, programmable |
| Input Subcarrier Amplitude Range | 15 mVpp to 4.0 Vpp |
| Maximum Safe Input | ± 35 VDC |
| FM Subcarrier Deviation Range | 0.5% to 50.0% of entered center frequency |
| Demodulation Mode | FM |
| Input Impedance Matching | 50, 75 and 10K Ohms shunted by 10 pF, selectable |

Demodulator Specifications

Output Filter Frequency Modes

There are 3 digital output filter frequency modes:

Analog Mode (Linear Data): The FIR filter is programmed to be flat within 0.1 dB in the programmed passband and -60 dB attenuation at 2 times the programmed cutoff frequency.

Digital Mode (PCM Data): The FIR filter is programmed to be monotonic in the passband with -3 dB attenuation at the programmed cutoff frequency and down -50 dB at 2.5 to 3.0 times the programmed cutoff frequency.

Bypass Mode (>1MHz Data): The digital and analog reconstruction filters are bypassed for maximum digital data throughput, up to 2.7 Mbps NRZL. The data frequency throughput is equal to the programmed deviation filter frequency.

Output Filter Frequency Range

Programmable from 1 Hz to 1 MHz with FM deviation ratios from 1 to 64 of the programmed deviation or from 1.5% to 50% of the subcarrier frequency

Output Linearity

Less than 0.05% of programmed full deviation bandwidth measured from the best 3 point straight line

Output Harmonic Distortion

All harmonic terms are below -56 dB for FM deviation ratios of 2 and -60 dB for FM deviation ratios >5

Output Impedance

1 k Ohm

Analog Output Level

Programmable from 1.0 Vpp to 10.0 Vpp with programmable offset from -5 VDC to +5 VDC

Analog Output Noise

Less than 10 mVRMS

Subcarrier Deviation Accuracy

0.0244% of the programmed center frequency (32 bit MNCO phase accumulator)

Linear Deviation Range

±125% of the programmed deviation

PCM Generator Specifications

PCM Output Format

NRZ-L or Randomized RNRZ-L PCM data and clock with 0° or 180° bit clock, program selectable

Word Size

16 bits per word, 32 bit sync pattern

Max Frame Size

2048 words

Output Bit Rate
Data Sample Rate

Sub-multiples of 80MHz clock, 20 Mbps max
2.5 to 5 or 5 to 10 samples per period based on the
programmed output filter frequency

Operation

The PCM Generator allows the user to build a PCM
frame containing data from selected digital
demodulator outputs available on the P2 connector.
The bit rate of the PCM output is determined by the
sample rates of each data channel. The sample rate
for each channel is determined by the programmed
output filter frequency.

Physical Specifications

VME Form Factor
Interface Connectors

32 bit VME 6U form factor
Subcarrier input, both demodulator analog outputs,
and PCM clock and data output signals are available
on BNC connectors.

Manufacturing

The design utilizes Surface Mount Technology
(SMT), manufactured with robotic assembly
techniques to IPC-610B Class 2 manufacturing
standards

Temperature Range

Operating: 0°C to 50°C
Storage: -20°C to 60°C

Power Consumption:

Less than 35 Watts total, for all supplies

Ordering Information

Syrinx-DualVME-01

Dual Digital FM Demodulator

1.3. Warranty

Ulyssix Technologies, Inc. warrants its products to be free from defects in material and workmanship, under normal use and service, for one year from the date of shipment to the original purchaser. The equipment must be returned transportation prepaid to the factory, and if found to be defective, at the Company's option, will be repaired or replaced free of charge and returned transportation prepaid. If inspection by Ulyssix does not disclose any defect in material or workmanship, Ulyssix's regular repair service charge will apply. This warranty does not extend to any products that have been subject to misuse, negligence, modifications or abnormal operating conditions or cover expendable items such as lamps, batteries, fuses, etc. Customer furnished equipment and hardware purchased for resale included in systems are covered by the original manufacturers warranty. Ulyssix makes no express or implied warranties beyond those described herein, and in no event will Ulyssix be responsible for consequential damages of any nature arising out of or connected with the use of its products.

1.4. Repair Service Charges

The minimum service charge for non-warranty repair of individual units, accomplished at our factory is \$250 per unit plus return shipping charges. Equipment must be shipped to the factory with transportation prepaid. Please call the Ulyssix Customer Service Department at 301-473-4217 for a return authorization number and shipping information. All units repaired will be warranted for 90 days from the date of the said repair.

Chapter 2 Installation

2.1 Product Identification

Every Syrinx-DualVME card is assigned a unique serial number before shipment from the factory. This number, as well as the unit's model and revision are clearly marked on the reverse side of the PC board. Refer to Figure 1.

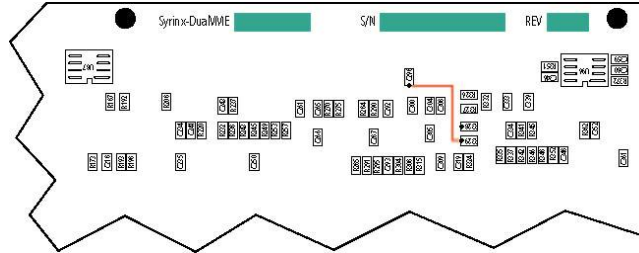


Figure 1 – Product Identification

2.1.1 Model Number

The model number of the Syrinx-DualVME card indicates which options are installed on that specific unit. Model number definitions are provided in the table below.

| Model | Description |
|-------------------|---|
| Syrinx-DualVME-01 | Standard Dual Digital Baseband FM Demodulator |

2.1.2 Serial Number

A unique serial number is assigned to each Syrinx-DualVME board. Reference this number to identify the specific unit during any communications with the factory.

2.1.3 Revision Number

The REV number indicates the assembly revision level of the unit.

2.2 Hardware Setup

2.2.1 General

The Syrinx-DualVME is a sophisticated electronic device. Damage can occur if the product is not handled and used properly. Care should be taken not to expose the unit to physical abuse, moisture, Electrostatic Discharge (ESD), or other potentially harmful conditions. Carefully unpack the board in an ESD safe location and check the product for physical damage from shipment. Factory installed modification wires and components will be secured to the board with adhesive to prevent damage. If there is any question about the condition of your board upon receipt, contact the factory.

2.2.2 Jumpers

Once the Syrinx-DualVME is unpackaged and no damage is apparent, check the unit to confirm that all required jumpers are present. Refer to Figure 2 for jumper locations. Three of the five jumpers required are factory set and require no alteration by the user. JP12 is used to set the input impedance of the card. See instructions below for setting JP12. JP4 or JP5 must be installed to set the number of address bits used during a transfer (24 or 32).

2.2.3 Setting Input Impedance

The Input Impedance of the Syrinx-DualVME is jumper selectable for 50, 75, or 10K Ohms. Cards are shipped from the factory with the jumper in the 10K Ohms position. The jumper selection sets the Input Impedance for both the Subcarrier Input (IN1) and the LRU Input (IN2). Special care must be taken in applications where the input signal is connected to multiple Syrinx-DualVME cards and the desired input impedance is either 50 or 75 Ohms. Install the jumper in the 50 or 75 Ohm position on **only** one Syrinx-DualVME board. Install all other jumpers in the 10K Ohm position. Significant input signal loading will occur if multiple cards have jumpers installed in the 50 or 75 Ohm locations. See Figure 3 below.

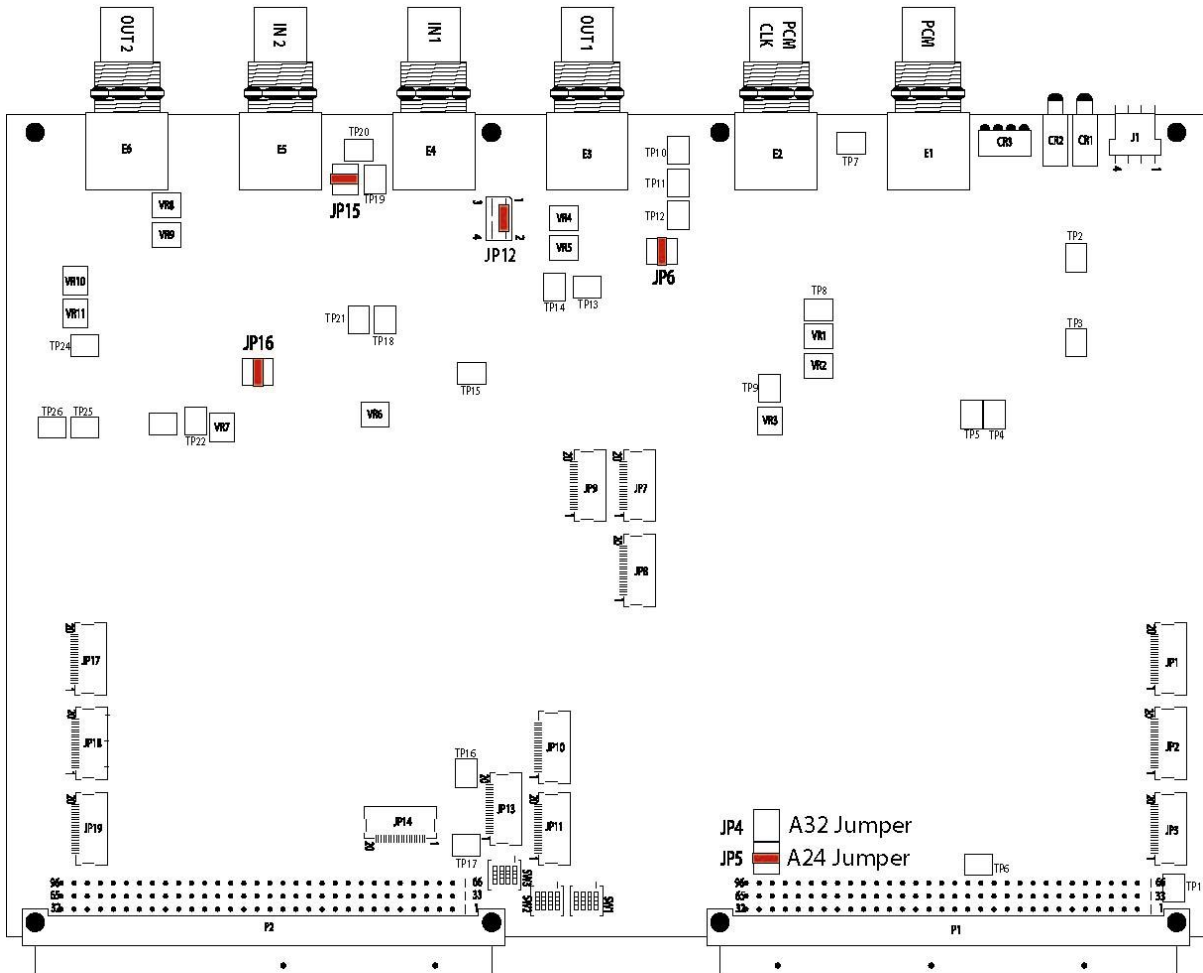


Figure 2 – Jumper Locations

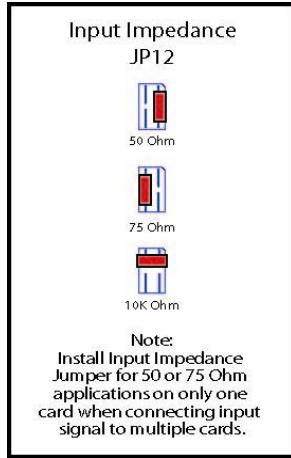


Figure 3 – Input Impedance

2.2.4 Setting the Syrinx-DualVME Board Base VME Address and ID

Each Syrinx-DualVME card must be assigned a unique base address by setting DIP switches SW1, SW2 and SW3 on the board. The Board ID LEDs (see Figure 5 below) reflect the value of SW1. Ulyssix recommends that you assign sequential board IDs (SW1) to the cards installed in your chassis and use SW2 and SW3 to offset this group of addresses if a conflict exists with other hardware in the chassis. Note that the Board IDs are numbered 0 through 15. Refer to Figure 5 and its associated table below to see the correlation between SW1 setting, Board ID, and the Board ID LEDs on the front panel.

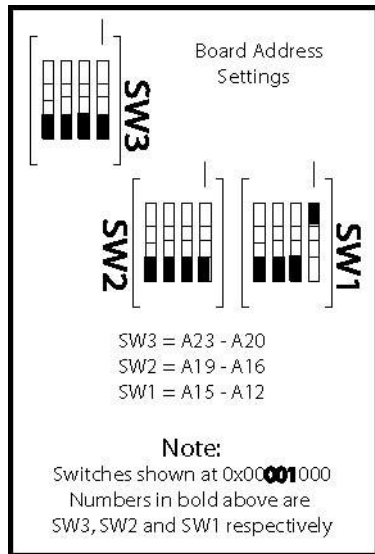


Figure 4 – Switch Settings

2.2.5 LED Indicators

LED Indicators on the front panel of the Syrinx-DualVME card provide identification and status for each card. The following sections describe the function of each LED.

2.2.6.1 Altera Download OK (RDY)

DSP algorithms are downloaded from on-board flash into Altera FPGAs upon power up of the Syrinx-DualVME. RDY, the Altera Download OK light, will illuminate after power up once the Altera FPGAs have successfully received the download. This LED will be illuminated during normal operation. If the Altera Download OK light is not illuminated after power up, contact the factory for assistance.

2.2.6.2 Demod Lock (LOCK)

The Demod Lock LED, LOCK, will illuminate green when the Syrinx-DualVME has detected data within the programmed Subcarrier and Deviation setup parameters. This LED will either illuminate green or flash green during normal operation. If the Lock LED is indicating NO LOCK when you expect it should be "locked", please verify that the board is not demodulating before contacting the factory for support.

2.2.6.3 Demod ID

A Demod ID number is set on each Syrinx-DualVME card by setting DIP Switches SW1, SW2, and SW3 (see section 2.2.4 above). The Demod ID LEDs give a binary representation of the Demod number for each card. Refer to the LED Indicator figure and table below to determine the Demod number.

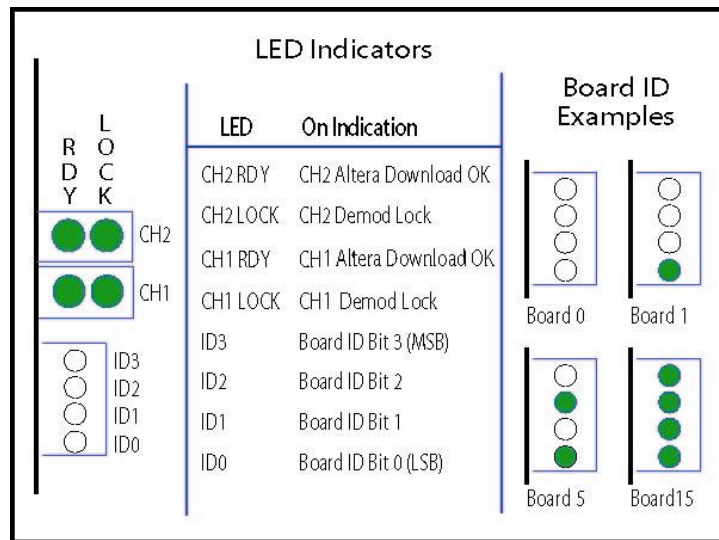


Figure 5 – LED Indicators

Note: 0 indicates LED off, 1 indicates LED on.

| SW1 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
|----------|---|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|
| ID 3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| ID 2 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| ID 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| ID 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| Board ID | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |

Board ID Table

2.2.6 Interconnections

Input and output connections are made to the Syrinx-DualVME through BNC connectors on the front panel. Refer to Figure 6 for connector identification.

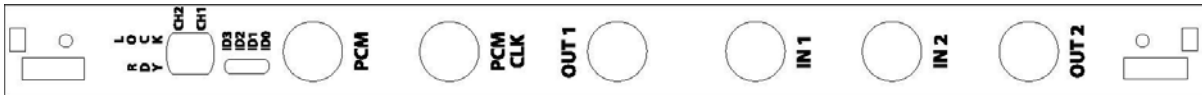


Figure 6 – Connections

2.2.6.1 Subcarrier Input (IN1)

Connect the signal to be demodulated to the Subcarrier Input Connector labeled IN1. Input Specifications for Syrinx-DualVME card are listed in the Specifications Section of this manual. The input impedance for the input to the board is jumper selectable for 50, 75 or 10K Ohms. See the Hardware Setup Section for details on how to select the input impedance.

2.2.6.2 Line Replacement Unit Input (IN2)

The Syrinx-DualVME card provides the user with the ability to select one of two connected inputs. This is typically used to connect a calibration signal to the demodulator to verify system integrity prior to a test. Connect the LRU input to the connector labeled IN2.

2.2.6.3 Output 1, Output 2

The Syrinx-DualVME has two FM demodulators per card. Throughout this manual these will be referred to as Channel 1 and Channel 2 and will correspond with the connectors labeled OUT1 and OUT2 respectively.

2.2.6.4 PCM Output

The Syrinx-DualVME card is equipped with a PCM frame generator that will create an NRZL or RNRZL data stream containing demodulated data from multiple channels within a system. The Syrinx-DualVME card identified as Board 0 will provide the PCM output for cards within the system.

2.2.6.5 PCM Clock Output

The PCM Clock output provides 0° or 180° bit clock for the PCM output, program selectable.

Chapter 3 Programming Operation

3.1 Programming Program Organization and Flow

This section of the manual describes the various hardware read and write register actions that must be performed to set up the SyrinxDualVME. The setup process is broken into 3 sections, system input write functions, individual demodulator channel write functions and then individual channel read status functions. By performing all of the following system input and channel write functions, the SyrinxDualVME card will function correctly. For reference, Chapter 4 has the complete description of each control register organized by address and Chapter 5 has examples of the control register write values for some standard IRIG demodulator frequency setups.

All control registers on the Syrinx-DualVME are written to as 16-bit unsigned or signed short values. To calculate many of the values, double variables are used. Please note in the following instructions where double variables are used and where integer variables are used.

3.1.1 System Input Write Functions

- System Preliminary Control Register setup
- Input Connection Selection
- Anti Alias Filter Setup
- Analog to Digital Converter (A/D) Clock Selection
- Auto Gain Control Enabling

3.1.2 Channel Write Functions

- Subcarrier Center Frequency Setup
- Subcarrier Deviation Frequency Setup
- Output Filter Frequency Setup
- Output Filter Mode
- Analog Output Offset
- Analog Output Gain Level
- Demod Lock LED Sensitivity

3.1.3 Channel Read Functions

- ASCII Signature Readback
- FPGA Configuration Programming Readback
- Demodulator Output Data Asynchronous Readback
- Demodulator Lock Status Readback
- Output Filter FIR Coefficient Verification Readback
- FIFO Output Data Synchronous Readback

3.2 Syrinx-DualVME System Write Register Functions

3.3.1 Preliminary Setup

It is good design practice to save each VME control register address in a static unsigned short value that can have each control bit set with an OR (!) process and clear the bit with an AND (&) process. To start, each value should be set to 0 in the software.

Next, the following registers are factory test control registers and must be set to the following values. Refer to address map and take care not to inadvertently change these register bits in other sections of your code.

Write to Register 98h, Bit 2 (MODOUT)

Set Bit 2 = 0

Write to Register C8h, Bit 3 (Mode)

Set Bit 3 = 0

Write to Register 100h, Bit 0 (PN24SEL)

Set Bit 0 = 0

Write to Register 498h, Bit 2 (MODOUT)

Set Bit 2 = 0

Write to Register 4C8h, Bit 3 (Mode)

Set Bit 3 = 0

Write to Register 528h, Bit 0 (AUTO AGC)

Set Bit 0 = 1

3.3.2 Input Connection Selection

The Syrinx-DualVME card allows the user to select 1 of 2 input connectors for the source of input signal to the demodulator. This allows the user software control to switch in a calibration signal to verify system operation prior to a test.

To select the source of input to the demodulator set INSEL as follows.

Write to Register D0h, Bits 8..7

To select Input 1 (IN1, Connector E4) Set Bit 8=0 and Bit 7=1

To select Input 2 (IN2, Connector E5) Set Bit 8=1 and Bit 7=0

Note: Refer to address map and take care not to inadvertently change other register bits.

3.3.3 Analog Front End

Both demodulator channels on the card share a common analog front end. The programming setup for the analog front end consists of setting the Anti-Alias filter frequency; the A/D Clock Frequency selection and enabling the auto gain control (AGC) circuit.

3.2.3.1 Anti-Alias Filter (AASEL 1..0)

The Syrinx-DualVME has two frequency ranges for anti-alias filtering. The same anti-alias filter will be applied to both channels on the card. Care should be taken to group channels on a given card that will be compatible with the same anti-alias filter. Also, the anti-alias filter should be chosen based on the channel with the higher upper band edge. Select the anti-alias filter for the required channel as follows.

Calculate the subcarrier upper band edge (UBE) by adding the Subcarrier Center Frequency (CF) to the Deviation Frequency. The UBE must be less than or equal to 3.5 MHz.

SubcarrierUpperBandEdge = SubcarrierCenterFrequency + SubcarrierDeviation;

if (SubcarrierUpperBandEdge > 14648.4375)

AASEL = 1; // Anti-aliasing filter = 3.5 MHz

else

AASEL = 2; // Anti-aliasing filter = 14.660 kHz

Write to Register D0h, Bits 10..9, (AASEL 1..0)

Write AASEL bit in the control register with the calculated value.

Note: Refer to address map and take care not to inadvertently change other register bits.

3.2.3.2 A/D Clock Frequency Select (CLKSEL)

The Syrinx-DualVME allows the user to select from two A/D clock frequencies. Typically the clock frequency choice is based on the upper band edge of the highest channel for the card. Select the A/D Clock frequency as follows:

Calculate the upper band edge (UBE) by adding the Subcarrier Center Frequency (CF) to the Deviation Frequency. The UBE must be less than 3.5 MHz.

```
if (SubcarrierUpperBandEdge > 14648.4375)
    CLKSEL = 0;          // A/D Clock frequency = 15 MHz
else
    CLKSEL = 1;          // A/D Clock frequency = 58.59375 kHz
```

Write to Register C8h, Bit 0

Write CLKSEL bit in the control register with the calculated value.

Note: Refer to address map and take care not to inadvertently change other register bits.

3.2.3.3 Auto Gain Control Enabling and Time Constant

The Auto Gain Control on the Syrinx-DualVME must be set for automatic mode as mentioned in the Preliminary Setup section. The AGC function is performed internally on the board and the VME controller does not have to do anything. The Gain and Offset DAC values can be monitored on the ODATA bus.

Write to Register 528h, Bit 0 (AUTO AGC)

Set bit 0 (AUTO AGC) = 1 Automatic mode

The Syrinx-DualVME has a selectable time constant for the AGC circuit. For most FM applications, setting the Time Constant to 1 for 12 msec is recommended. For some applications with subcarrier rates above 2 MHz, the 0.12 msec time constant may improve demodulator performance. For subcarriers below 1 kHz, a slower time constant may improve demodulator performance.

Write to Register 528h, Bits 7..6 (AGC Time Constant)

Set bits 7..6 to 1 = 0 AGC Time Constants = 0.12 msec

Set bits 7..6 to 1 = 1 AGC Time Constants = 12 msec (recommended)

Set bits 7..6 to 1 = 2 AGC Time Constants = 102 msec

Set bits 7..6 to 1 = 3 AGC Time Constants = 408 msec

Note: Refer to address map and take care not to inadvertently change other register bits.

Read AGC DAC values (factory test purpose only)

Write to Register 500h, Bits 12..11

Set Bit 12 (DEMODREN) = 0

Set Bit 11 (LOCKREN) = 0

Write to Register 500h, Bit 10

Set DACREN = 0 To Enable Read of AGC Gain DAC value

Set DACREN = 1 To Enable Read of AGC Offset DAC value

Note: Refer to address map and take care not to inadvertently change other register bits.

Read Register 418h, Bits 7..0

DACx [7..0] = Value of Gain (DACA) or Offset (DACB) DAC

Note: Two read cycles are required because the data is double buffered in the control register. Ignore the first reading.

3.3.4 Subcarrier Center Frequency

The frequency range of the Syrinx-DualVME is 250 Hz to 3.5 MHz. Therefore, the subcarrier center frequency plus the deviation must be less than 3.5 MHz and the subcarrier center frequency minus the deviation must be greater than 250 Hz.

Programming the Subcarrier Center Frequency requires multiple calculations and writes. These calculations include calculating and setting the A2Ddivisor, Multiplex Decimations and MNCO phase step size. The following sections explain the calculation for each parameter.

3.2.4.1 A/D Clock Frequency Divisor

The A/D Clock Frequency Divisor value is needed for the MNCO phase step calculation.

```
if (SubcarrierUpperBandEdge > 14648.4375)
    A2DDivisor = 0;          // A/D Clock frequency = 15 MHz
else
    A2DDivisor = 8;        // A/D Clock frequency = 58.59375 kHz
```

Save this value for later use.

3.2.4.2 Multiplex Decimations (MUXSEL 3..0)

In order to calculate and set the number of Multiplex Decimations, first a calculation of the current clock frequency to the A/D clock is necessary. The ratio value is determined as follows:

```
if (AASEL == 1)
    ratio = 3.75e6 / SubcarrierUpperBandEdge;
else
    ratio = 14648.4375 / SubcarrierUpperBandEdge;
```

Calculate the proper number of decimations (muxsel) with the following formula:

```
for (muxsel = 0; muxsel <= 8; muxsel++)
{
    if ((pow(2.0, muxsel) < ratio) && (pow(2.0, muxsel + 1) > ratio))
        break;          //proper number of decimations
}
```

Write to Register 98h (Channel 1) or 498h (Channel 2), Bits 11..8, (MUXSEL 3..0)

Load MUXSEL with the binary value for the proper number of decimations.

Note: Refer to address map and take care not to inadvertently change other register bits.

3.2.4.3 MNCO Phase Step (PHASESTEP 31..0)

The MNCO phase step calculation is used to set the complex downconverter to the correct frequency. The phase step value is a 32 bit signed long value that is written to the SyrinxDualVME card in two 16 bit write sequences. The following are the calculations and write sequences.

Calculate

Downclock = 15e6 / pow(2.0, A2DDivisor + MUXSEL); // This is the downconverted clock rate

```
(long)PhaseStep = (long)((((SubcarrierCenterFrequency / Downclock) * pow(2.0, 32.0)) + 0.5);
```

Write to Register 80h (Channel 1) or 480h (Channel 2), Bits 15..0

MSWord of PhaseStep[31..16] - (16 bits)

Write to Register 88h (Channel 1) or 488h (Channel 2), Bits 15..0

LSWord of PhaseStep[15..0] - (16 bits)

3.3.5 Subcarrier Deviation Frequency

The Subcarrier Deviation Frequency range is from 0.5% to 50.0% of the programmed center frequency. Care must be taken to be certain that the subcarrier center frequency plus deviation must be less than 3.5 MHz and the subcarrier center frequency minus the deviation must be greater than 250 Hz.

Programming the Subcarrier Deviation Frequency requires multiple calculations and register writes. These calculations include calculating and setting the input filter number of decimations both coarse and fine settings, the deviation complex offset, the sample clock for the demodulation process and the scale factor for the conversion from phase to amplitude. The following sections explain the calculation for each parameter.

3.2.5.1 Deviation Filter Settings (DECSEL 3..0, FILSEL 1..0)

The bandpass filter algorithm for the digital demodulator is performed by feeding the output of the complex downconverters into a DSP based decimation low pass filter (coarse setting) and then a following FIR filter (fine setting). The user entered subcarrier deviation value sets the filters settings. The following are the calculations and write sequences.

Calculate

```
dev5 = 5.0 * SubcarrierDeviation;  
dev10 = 10.0 * SubcarrierDeviation;  
for (decsel = 0; decsel <= 8; decsel++)  
{  
    if ((Downclock / pow(2.0, decsel) > dev5) && ((Downclock / pow(2.0, decsel)) < dev10)  
        break;           //correct number of input decimations  
}
```

Write to Register C8h (Channel 1) or 4C8h (Channel 2), Bits 11..8

Load DECSEL with the binary value for correct input decimations.

Next, the FILSEL deviation filter fine selection is calculated and written.

Calculate

```
Demodclock = Downclock / pow(2.0, decsel);           // demod sample clock rate  
if (((SubcarrierDeviation < ( 0.13 * Demodclock)) && (SubcarrierDeviation >= (0.10 * Demodclock)))  
    filsel = 0;  
if (((SubcarrierDeviation < ( 0.16 * Demodclock)) && (SubcarrierDeviation >= (0.13 * Demodclock)))  
    filsel = 1;  
if (((SubcarrierDeviation < ( 0.19 * Demodclock)) && (SubcarrierDeviation >= (0.16 * Demodclock)))  
    filsel = 2;  
else  
    filsel = 3;
```

Write to Register D0h (Channel 1) or 4D0h (Channel 2), Bits 6..5

Load FILSEL with the calculated value.

Note: Refer to address map and take care not to inadvertently change other register bits.

3.2.5.2 Deviation Complex Offset Setting (DECOFF 3..0)

The deviation complex offset setting is based on the calculation of the coarse decimation filter setting DECSSEL.

Calculate

```
index[9] = {2, 2, 3, 4, 5, 6, 7, 8, 9};  
decoff = index[decsel];
```

Write to Register C8h (Channel 1) or 4C8h (Channel 2), Bits 15..12

Load DECOFF with the binary value for correct input decimations.

Note: Refer to address map and take care not to inadvertently change other register bits.

3.2.5.3 FCLOCK Select (FCLKSEL 3..0)

The sample rate of the data moving from the input deviation filter through the digital demodulator is dependent on the DECSSEL and MUXSEL values previously determined.

Calculate

```
TotalDecimate = decsel + muxsel;  
if (A2DDivisor == 0) //UBE > 14648.4375Hz  
{  
    if (TotalDecimate > 0)  
        fclksel = TotalDecimate - 1;  
    else  
        fclksel = 0;  
}  
else  
    fclksel = 7 + TotalDecimate;
```

Write to Register E0h (Channel 1) or 4E0h (Channel 2), Bits 3..0

Load FCLKSEL with the binary value of fclksel.

Note: Refer to address map and take care not to inadvertently change other register bits.

3.2.5.4 Deviation Select (DEVSEL 1..0) and Deviation Scalar (DEVSCALAR 15..0)

To convert from phase to amplitude in the digital demodulator, you must calculate and write the deviation scalar and pipeline select values. These scale factors scale the demodulator output to 555h for 100% deviation, 000h for 0% deviation and aaah for -100% deviation.

Calculate

```
ftmp = ((SubcarrierDeviation / Demodclock) * 2.0 * 3.14159) * 512.0;  
ftmp = 1365.0 / ftmp;  
if ((0.0 <= ftmp) && (ftmp < 1.0))  
{  
    devsel = 0;  
}  
else if ((1.0 <= ftmp) && (ftmp < 2.0))  
{  
    devsel = 1;  
    ftmp /= 2.0;  
}  
else if ((2.0 <= ftmp) && (ftmp < 4.0))  
{  
    devsel = 2;  
    ftmp /= 4.0;
```

```

}
else if ((4.0 <= ftmp) && (ftmp < 8.0))
{
    devsel = 3;
    ftmp /= 8.0;
}
else
{
    devsel = 3;
    ftmp = 0.9999;
}
devscalar = (unsigned short)(((ftmp * 32768.0) + 0.5) * -1.0);

```

Write to Register C8h (Channel 1) or 4C8h (Channel 2), Bits 2..1

Load DEVSEL with the calculated value.

Note: Refer to address map and take care not to inadvertently change other register bits.

Write to Register C0h (Channel 1) or 4C0h (Channel 2), Bits 15..0

Load DEVSCALAR with the calculated value.

3.3.6 Output Filter Frequency Setup

The output filter frequency of the digital demodulator is programmable with a maximum frequency equal to the input deviation filter setting and a minimum frequency equal to 1/64 of the input deviation filter setting. To program the Output Filter Frequency the following items must be calculated and written to the hardware registers: the type of Output Filter (analog, digital or OFF), the number of output decimations to be used by the Output Filter, the table index into the FIR Output Filter coefficient, loading the FIR coefficients and the analog reconstruction filter fine and coarse setting.

3.2.6.1 Output Filter Type (OUTSEL)

The digital FIR filter and analog reconstruction filter have 3 different selections, analog, digital or OFF. The hardware allows the user to bypass both the digital and analog reconstruction filter separately. Normally, if the filter is set to OFF, both filters should be bypassed.

The OUTSEL bit disables or bypasses the digital FIR filter.

Write to Register 308h (Channel 1) or 708h (Channel 2), Bit 1

| | |
|------------------------|-----------------------------------|
| Set OUTSEL (bit 1) = 0 | Output Filter enabled |
| Set OUTSEL (bit 1) = 1 | Output Filter disabled (bypassed) |

Note: Refer to address map and take care not to inadvertently change other register bits.

The RECFIL bit is used to enable or disable (bypasses) the analog reconstruction filter. When the output filter type is OFF, the reconstruction filter is disabled. When the type is ANALOG or DIGITAL, the reconstruction filter is enabled.

Write to Register D0h (Channel 1) or 4D0h (Channel 2), Bit 11

| | |
|-------------------------|--|
| Set RECFIL (bit 11) = 0 | Analog Reconstruction Filter disabled (bypassed) |
| Set RECFIL (bit 11) = 1 | Analog Reconstruction Filter enabled |

Note: Refer to address map and take care not to inadvertently change other register bits.

3.2.6.2 Output Filter Decimations (OUTDEC 2..0)

The number of output decimations ranges from 0 to 6. During this calculation the output Outputclock is determined which will be used in future calculations.

Calculate

```
if (OutputFilterType == OFF)
{
    outdec = 0; //if Output Filter Mode off, decimations equals zero
    Outputclock = Demodclock; // output clock is Demodclock
}
dev5 = 5.0 * OutputFilterFrequency;
dev10 = 10.0 * OutputFilterFrequency;
for (outdec = 0; outdec <= 6; outdec++)
{
    clk = pow(2.0, outdec);
    Outputclock = Demodclock / clk;
    if ((Outputclock > dev5) && (Outputclock <= dev10))
        break; //good value
}
}
```

Write to Register C8h (Channel 1) or 4C8h (Channel 2), Bits 6..4

Load OUTDEC [2..0] with the calculated value.

Note: Refer to address map and take care not to inadvertently change other register bits.

3.2.6.3 Output Filter Coefficients (RAM 11..0)

The 3 possible types of Output Filters are described below. The 16 bit short analog filter coefficients are stored in the acoef table listed in this section. The 16 bit short digital filter coefficients are stored in the dcoef table also list below. Both tables use the same indexing algorithm to choose the correct coefficient for the programmed output filter frequency. This table index (tblidx) calculation is shown below.

Analog Mode (Linear Data): The FIR filter is programmed to be flat within 0.1 dB in the programmed passband and -60 dB attenuation at 2 times the programmed output filter cutoff frequency.

Digital Mode (PCM Data): The FIR filter is programmed to be monotonic in the passband with -3 dB attenuation at the programmed cutoff frequency and down -50 dB at 2.5 to 3.0 times the programmed output filter cutoff frequency.

OFF Mode (>1MHz Data): The digital and analog reconstruction filters are bypassed for maximum digital data throughput, up to 2.7 Mbps NRZL. The data frequency throughput is equal to the programmed deviation filter frequency.

Calculate

```
if ((OutputFilterFrequency < (0.20 * Outputclock)) && (OutputFilterFrequency >= (0.19 * Outputclock)))
    tblidx = 9;
if ((OutputFilterFrequency < (0.19 * Outputclock)) && (OutputFilterFrequency >= (0.18 * Outputclock)))
    tblidx = 8;
if ((OutputFilterFrequency < (0.18 * Outputclock)) && (OutputFilterFrequency >= (0.17 * Outputclock)))
    tblidx = 7;
if ((OutputFilterFrequency < (0.17 * Outputclock)) && (OutputFilterFrequency >= (0.16 * Outputclock)))
    tblidx = 6;
if ((OutputFilterFrequency < (0.16 * Outputclock)) && (OutputFilterFrequency >= (0.15 * Outputclock)))
    tblidx = 5;
if ((OutputFilterFrequency < (0.15 * Outputclock)) && (OutputFilterFrequency >= (0.14 * Outputclock)))
    tblidx = 4;
if ((OutputFilterFrequency < (0.14 * Outputclock)) && (OutputFilterFrequency >= (0.13 * Outputclock)))
    tblidx = 3;
if ((OutputFilterFrequency < (0.13 * Outputclock)) && (OutputFilterFrequency >= (0.12 * Outputclock)))
```

```

tblidx = 2;
if ((OutputFilterFrequency < (0.12 * Outputclock)) && (OutputFilterFrequency >= (0.11 * Outputclock)))
    tblidx = 1;
if ((OutputFilterFrequency < (0.11 * Outputclock)) && (OutputFilterFrequency >= (0.10 * Outputclock)))
    tblidx = 0;

```

Write to Registers 200h – 278h (Channel 1), Bits 11..0 or 600h – 678h (Channel 2), Bits 11..0 with address spacing of 8h between each coefficient value

The following is the array for the analog mode FIR digital filter coefficients.

```

unsigned short acoef[10][16] =
{
{0x002, 0x000, 0xff8, 0xfec, 0xfea, 0x002, 0x02e, 0x04c, 0x02e, 0xfc7, 0xf51, 0xf41, 0xffc, 0x180, 0x341, 0x470},
{0x003, 0x008, 0x009, 0xffc, 0xfe5, 0xfdd, 0xfff, 0x03f, 0x05f, 0x01b, 0xf81, 0xf17, 0xf8e, 0x128, 0x34e, 0x4da},
{0xfff, 0x000, 0x006, 0x00b, 0x000, 0xfe6, 0xfdb, 0x006, 0x051, 0x05c, 0xfda, 0xf23, 0xf30, 0x0ba, 0x34a, 0x54b},
{0xfff, 0xffc, 0xfff, 0x00b, 0x011, 0xffb, 0xfd5, 0xfdb, 0x02d, 0x077, 0x028, 0xf49, 0xef0, 0x055, 0x33a, 0x5ab},
{0x000, 0xfff, 0xffc, 0xffe, 0x00c, 0x013, 0xff4, 0xfca, 0xfce, 0x060, 0x071, 0xf9c, 0xecd, 0xfda, 0x312, 0x616},
{0x001, 0x002, 0xfff, 0xff7, 0xffe, 0x016, 0x013, 0xfd9, 0xfc1, 0x02f, 0x097, 0xff4, 0xeca, 0xf6c, 0x2e0, 0x676},
{0xfff, 0x000, 0x004, 0xfff, 0xff2, 0xffc, 0x022, 0x009, 0xfb7, 0xfdf, 0x08e, 0x060, 0xfef4, 0xef5, 0x291, 0x6e4},
{0x000, 0xfff, 0x003, 0x003, 0xff7, 0xff4, 0x017, 0x01f, 0xfcc, 0xfbb, 0x06b, 0x091, 0xf24, 0xeb9, 0x256, 0x724},
{0x001, 0x000, 0xffd, 0x002, 0x009, 0xff4, 0xfed, 0x028, 0x019, 0xf9e, 0xff7, 0x0d0, 0xfb6, 0xe51, 0x1bb, 0x7ae},
{0x000, 0x001, 0xfff, 0xffd, 0x008, 0x003, 0xfe5, 0x00d, 0x038, 0xfbb, 0xfb7, 0x0c5, 0x01, 0xe36, 0x15b, 0x7f5},
};

```

The following is the array for the digital mode FIR digital filter coefficients.

```

unsigned short dcoef[10][16] =
{
{0x001, 0x004, 0x006, 0x002, 0x000, 0x00a, 0x013, 0x004, 0xff5, 0x017, 0x045, 0x019, 0xfd1, 0x07f, 0x28d, 0x48b},
{0x000, 0x005, 0x00b, 0x005, 0xff3, 0xff9, 0x025, 0x028, 0xfe0, 0xfd1, 0x04c, 0x077, 0xfcf, 0xfe6, 0x24f, 0x53a},
{0x000, 0x003, 0x008, 0x004, 0xff9, 0xfff, 0x01b, 0x018, 0xfe6, 0xfed, 0x04e, 0x050, 0xfb6, 0x003, 0x26e, 0x52e},
{0x008, 0x00b, 0xff3, 0xfeb, 0x022, 0x02f, 0xfdb, 0xfcf, 0x034, 0x03f, 0xffd, 0x004, 0xfe8, 0x010, 0x248, 0x560},
{0x006, 0x009, 0xffa, 0xff4, 0x011, 0x01e, 0xff7, 0xfe8, 0x00b, 0x021, 0x02b, 0x01d, 0xfb8, 0xffe, 0x266, 0x563},
{0x005, 0x008, 0xff9, 0xff7, 0x01d, 0x012, 0xfd3, 0x004, 0x055, 0xfe6, 0xfb5, 0x082, 0x051, 0xf63, 0x1b3, 0x624},
{0xfff, 0x002, 0x009, 0x000, 0xff7, 0x00e, 0x00d, 0xff4, 0x010, 0x00d, 0xfed, 0x04e, 0x029, 0xf7b, 0x1c3, 0x631},
{0xfff, 0x002, 0x007, 0xffd, 0xffc, 0x015, 0x000, 0xfea, 0x029, 0x012, 0xfc4, 0x056, 0x059, 0xf54, 0x18a, 0x674},
{0xffe, 0x002, 0x00c, 0xffa, 0xff3, 0x023, 0x008, 0xfc9, 0x034, 0x040, 0xf92, 0x034, 0x0af, 0xf3f, 0x123, 0x6c8},
{0x000, 0x002, 0x005, 0x000, 0xffc, 0x00f, 0x006, 0xfe8, 0x021, 0x021, 0xfb9, 0x043, 0x07c, 0xf3e, 0x14b, 0x6bd},
};

```

In order to be able to write the coefficients to the hardware the addressing bits must be set in the hardware. Before starting the coefficients writes, RAMSEL must be set to 0.

Write to Register 308h (Channel 1) or 708h (Channel 2), Bit 0

Set RAMSEL (bit 0) = 0 Allow VME bus to address the FIR Coefficient RAM
Set RAMSEL (bit 0) = 1 Allow internal counter addressing for real mode FIR usage

After completion of writing the coefficients, set the RAMSEL to 1 for internal addressing

Note: Refer to address map and take care not to inadvertently change other register bits.

Sample code for writing to the FIR filter coefficients RAM:

```

TurnBitOff(<RAMSEL control register>, RAMSEL);
for (i = 0, j = 0; i < 0x10; i++)
{
    addr = (unsigned short)(j + FIR_FILTER_WRITE_START_REG);
    if (OutputFilterMode == ANALOG)

```

```

        WriteRegister(addr, acoef[tblidx][i]);
else
        WriteRegister(addr, dcoef[tblidx][i]);
j += 0x8;
}
TurnBitOn (<RAMSEL control register>, RAMSEL);

```

3.2.6.4 Analog Reconstruction Filter coarse (RECON 2..0) and fine (RECONBSD 7..0) settings

The digital demodulator output data is converted to analog form using a 12-bit digital to analog converter (DAC) that is sampled with a clock running at output clock frequency. Since the clock used by the DAC changes with different programming, the analog reconstruction filter must be adjusted.

Calculate

```

if (OutputFilterFrequency > 45000.0)
{
    recon = 0;
    res = ((1000000.0 - 45000.0) / 128.0);
    freconbsd = ((OutputFilterFrequency - 45000.0) / res);
    freconbsd += 127.0;
    reconbsd = (unsigned short)freconbsd;
}
else if (OutputFilterFrequency > 4000.0)
{
    recon = 1;
    res = ((45000.0 - 4000.0) / 124.0);
    freconbsd = ((OutputFilterFrequency - 4000.0) / res);
    freconbsd += 131.5;
    reconbsd = (unsigned short)freconbsd;
}
else if (OutputFilterFrequency > 400.0)
{
    recon = 3;
    res = ((4000.0 - 400.0) / 126.0);
    freconbsd = ((OutputFilterFrequency - 400.0) / res);
    freconbsd += 129.5;
    reconbsd = (unsigned short)freconbsd;
}
else // up to 400Hz
{
    recon = 7;
    res = ((400.0 - 10.0) / 111.0);
    freconbsd = ((OutputFilterFrequency - 10.0) / res);
    freconbsd += 120.0;
    reconbsd = (unsigned short)freconbsd;
}

```

Write to Register D0h (Channel 1) or 4D0h (Channel 2), Bits 4..2

Load RECON [2..0] with the calculated value. The value should be one of the following:

- 000 = OutputFilterFrequency frequencies from 45 kHz to 1 MHz
- 001 = OutputFilterFrequency frequencies from 4 kHz to 45 kHz
- 011 = OutputFilterFrequency frequencies from 400 Hz to 4 kHz
- 111 = OutputFilterFrequency frequencies from 1 Hz to 400 Hz

Write to Register 40h (Channel 1) or 440h (Channel 2), Bits 7..0

Load RECONBSD [7..0] with the calculated value. This value is an unsigned short form from 0x0000 to 0x00ff to control the reconstruction filter fine tune DAC.

Note: Refer to address map and take care not to inadvertently change other register bits.

3.2.6 Analog Output Offset (AOUTPUT 7..0)

The analog output offset level is programmable from –5 VDC to +5 VDC.

Calculate

```
res = (5.0 / 128.0); // DAC resolution
ftmp = (AnalogOutputOffset / res) * 0.8673; // 85% full scale
ftmp += 128.0; // set to bipolar
aoutput = (unsigned short)ftmp;
```

Write to Register D0h(Channel 1) or 4D0h (Channel 2), Bit 0

Set OUTDAC A/B to 1 to make Analog Output Offset active.

Write to Register 48h(Channel 1) or 448h (Channel 2), Bits 7..0

Load OUTPUT BSD 7..0 with AOUTPUT.

Write to Register D0h(Channel 1) or 4D0h (Channel 2), Bit 14

Drop _LDACOUT from logic 1 to logic 0 to load the OUTPUT BSD value into the DAC.
Return _LDACOUT to 1 to complete the load.

Note: Refer to address map and take care not to inadvertently change other register bits.

3.3.7 Analog Output Gain (AGAIN 7..0)

The analog output gain is programmable from 1.0 to 10.0 Vpp in 1.0 Vpp increments.

Calculate

```
short lut[10] = {0x5c,0x89,0xa3,0xb5,0xc3,0xce,0xd8,0xe0,0xe7,0xee};
// above array corresponds to 1Vpp – 10Vpp output level in 1Vpp increments
// i.e 0x5c = 1Vpp , 0xc3 = 5Vpp and 0xee = 10Vpp
```

Write to Register D0h(Channel 1) or 4D0h (Channel 2), Bit 0

Set OUTDAC A/B to 0 to make Gain active.

Write to Register 48h(Channel 1) or 448h (Channel 2), Bits 7..0

Load OUTPUT BSD 7..0 with the lut[] array value from above.

Write to Register D0h(Channel 1) or 4D0h (Channel 2), Bit 14

Drop _LDACOUT from logic 1 to logic 0 to load the OUTPUT BSD value into the DAC.
Return _LDACOUT to 1 to complete the load.

Note: Refer to address map and take care not to inadvertently change other register bits.

3.3.8 Demod Lock Indicator, (DMLOCK)

The Demod Lock feature indicates that energy has been detected in the programmed channel frequency range. A value of the energy present (LOCK [11..0]) is compared to a threshold value (LOCKREG [11..0]), and the result determines the state of DMLOCK.

Set Threshold

Write to Register 108h (Channel 1) or 508h (Channel 2), Bits 11..0

Load LOCKREG, the threshold value for the LOCK indicator, with a value between 0 and 200h. For most applications, the value of 100h is a nominally good value to store.

Read DMLOCK status

Write to Register 100h (Channel 1) or 500h (Channel 2), Bits 12..11

Set bit 12 (DEMODREN) = 0

Set bit 11 (LOCKREN) = 1

Note: Refer to address map and take care not to inadvertently change other register bits.

Read Register 118h (Channel 1) or 518h (Channel 2), Bit 12

DMLOCK = 1 indicates "LOCK" status

DMLOCK = 0 indicates "NO LOCK" status

Note: Two read cycles are required because the data is double buffered in the control register. Ignore the first reading.

3.3 Syrinx-DualVME System Read Register Functions

The SyrinxDualVME card has many readback registers to allow the user to verify card startup performance as well as read back demodulator status. All read values on the SyrinxDualVME are double buffered which means 2 reads must be performed with the first reading being ignored.

3.3.1 ASCII Signature Readback

The ASCII Signature Readback register is available to perform very basic board level communication checks. Registers 780h to 7B8h are loaded with ASCII characters that can be read by the VME controller. This readback verifies the VME bus is communicating cleanly with the SyrinxDualVME as well as that the SyrinxDualVME is up and running successfully.

Read ASCII Signature Register, Bits 7..0

| Register | ASCII Character | Binary Value |
|----------|-----------------|--------------|
| 780h | S | 01010011 |
| 788h | Y | 01011001 |
| 790h | D | 01000100 |
| 798h | U | 01010101 |
| 7A0h | A | 01000001 |
| 7A8h | L | 01001100 |
| 7B0h | 1 | 00110001 |
| 7B8h | NULL | 00000000 |

Note: Two read cycles are required because the data is double buffered in the control register. Ignore the first reading.

3.3.2 Tape Speed Compensation or Config Done (TSC/CONF_DONE)

If TSC is enabled, this register is driven by a demodulator used as a reference channel and multiplied by DEV_CNST [15..0] for Tape Speed Compensation input to data channels.

If CONF_DONE is enabled, this register is driven by the configuration done bit for the 11 Altera FPGAs on the board. This feature allows the user to poll the Altera's and confirm that they were properly initialized.

Write to Register 98h, Bit 1

To Select TSC

Set Bit 1 = 1

To select CONF_DONE

Set Bit 1 = 0

For Tape Speed Compensation

Read Register A0h, Bits 11..0

TSC reference channel data multiplied by DEV_CNST.

Note: Two read cycles are required because the data is double buffered in the control register. Ignore the first reading.

FOR ALTERA CONF_DONE

Read Register A0h, Bits 11..0

Read the configuration done bits per the following table

| <u>Register Bit</u> | <u>Reference Designator</u> | <u>Board Channel</u> |
|---------------------|-----------------------------|----------------------|
| 0 | U23 | 1 |
| 1 | U7 | 1 |
| 2 | U20 | 1 |
| 3 | U1 | 1 |
| 4 | U10 | 1 |
| 5 | U42 | 2 |
| 6 | U60 | 2 |
| 7 | U49 | 2 |
| 8 | U66 | 2 |
| 9 | U52 | 2 |
| 10 | U30 | 1 |

Note: Two read cycles are required because the data is double buffered in the control register. Ignore the first reading.

3.3.3 Demodulated Data Asynchronous Readback (OUTFIL)

This register provides asynchronous readback of the demodulated data in two's complement format. The value is formatted in the demodulator that -100% deviation is aaaah, 0% deviation is 0h and +100% deviation is 5555h. Read the data value as follows:

Read Register 300h (Channel 1) or 700h (Channel 2), Bits 15..0

OUTFIL = 16 bit value of demodulated data.

Note: Two read cycles are required because the data is double buffered in the control register. Ignore the first reading.

3.3.4 Demod Lock Value and Status Readback (LOCK, DMLOCK)

The function of the Demod lock indicator (DMLOCK) feature of the board is explained in the Write Register section of this manual. To read the value of energy present (LOCK) or the status of Demod Lock (DMLOCK), do the following:

Write to Register 100h (Channel 1) or 500h (Channel 2), Bits 12..11

Set bit 12 (DEMODREN) = 0

Set bit 11 (LOCKREN) = 1

Note: Refer to address map and take care not to inadvertently change other register bits.

Read Register 118h (Channel 1) or 518h (Channel 2), Bit 12

DMLOCK = 1 indicates "LOCK" status

DMLOCK = 0 indicates "NO LOCK" status

Read Register 118h (Channel 1) or 518h (Channel 2), Bits 11..0

LOCK = 12 bit value of the sum of 8 samples of SINDEC data used to determine lock status.

Note: Two read cycles are required because the data is double buffered in the control register. Ignore the first reading.

3.3.5 Output FIR Filter Coefficient Readback

To read the coefficients for the Output FIR Filter that are currently loaded into registers 200h – 278h (channel 1) or 600h – 678h (channel 2), do the following:

Read Register 280h – 2F8h (Channel 1) or 680h - 6F8h (Channel 2), Bits 11..0

RAMCOEFFx = 12 bit coefficient value

Note: Two read cycles are required because the data is double buffered in the control register. Ignore the first reading.

3.3.6 FIFO Readback

The SyrinxDualVME card has a 1024x32 bit buffered FIFO output that is used to capture the digital demodulator data directly across the VME bus. An FFT algorithm to display the frequency content of the output data can use this data or the data can be directly sent to the host computer for storage.

The data is stored in the FIFO in a 32 bit configuration in the following format:

Bits[31..16] are all associated with one demodulator word and Bits[15..0] are associated with either the next or previous demodulator word.

Bit 31/15 – FIFO status register where 1 indicates either the FIFO full or empty flag is set

Bits[30..28]/[14..12] – internal counter, which counts from 0 to 7 and then wraps again to help keep track of each value read.

Bits[27..16]/[11..0] – 12 2's complement demodulator output data.

To start the FIFO read process, the FIFO must be reset.

Write to Register 140h (Channel 1) or 540h (Channel 2), Bit 1

Set Bit 11 (_FIFORST) = 0 which sets the FIFO reset of the address head and tail pointer

Set Bit 11 (_FIFORST) = 1 which turns off the reset the FIFO address head and tail pointers

Next, the FIFO Full flag must be polled to see that the FIFO is full of data.

Read Register 168h (Channel 1) or 568h (Channel 2) Bit 3

_FIFOFF = 0 indicates the FIFO is full and data is ready to be read out.

_FIFOFF = 1 indicates the FIFO is still filling with data.

Note: Two read cycles are required because the data is double buffered in the control register. Ignore the first reading.

Reading the FIFO is done by performing a 32 bit read of the FIFO.

Read Register 148h (Channel 1) or 548h (Channel 2) Bits 31..0

Continuous synchronous values from the FIFO can be verified by looking at the counter bits attached to the top nibble of each FIFO value to be certain a continuous count is progressing.

After the read is performed, the FIFO is ready to be reset and restart the entire process.

Another feature that can be performed with the FIFO is a direct data logging function. This is done by resetting the FIFO but this time, not waiting for the FIFO to be full. Start reading from

the FIFO being certain that the FIFO isn't either FULL or EMPTY. If the FIFO is empty, wait until data is moved into the FIFO and continue reading. If the FIFO is full, data is being lost and the process needs to be halted.

3.3.7 AGC DAC Value Readback (DAC A, DAC B)

An internal FPGA state machine controls the auto gain control circuit. For system troubleshooting capability, readback registers are available.

Write to Register 500h, Bits 12..11

Set Bit 12 (DEMODREN) = 0

Set Bit 11 (LOCKREN) = 0

Write to Register 500h, Bit 10

Set DACREN = 0 To Enable Read of AGC Gain DAC value

Set DACREN = 1 To Enable Read of AGC Offset DAC value

Note: Refer to address map and take care not to inadvertently change other register bits.

Read Register 518h, Bits 7..0

DACx [7..0] = Value of Gain (DACA) or Offset (DACB) DAC

Note: Two read cycles are required because the data is double buffered in the control register. Ignore the first reading.

Chapter 4 SyrnxDualVME Address Map

4.1 System Address Map

| Reg | R/W | Ch | Bits | Description |
|-----|-----|----|--------|--|
| 00h | W | | 8 | INTCLR, Interrupt Clear Enable 0 = Inactive 1 = Interrupt Clear active, resets interrupts (Note: System Clear, CLR = 1, also reset interrupts.) |
| | | | 7..5 | INT2SEL [2..0], 3 bits used to decode interrupt (IRQ[7..1]). Logically "OR'ed" with INT1SEL [2..0] |
| | | | 4..2 | INT1SEL [2..0], 3 bits used to decode interrupt (IRQ[7..1]). Logically "OR'ed" with INT2SEL [2..0] |
| | | | 1 | FIFO2SEL, Select line for FIFO2INT [1..0] 0 = Selects _FIFO2INT0 1 = Selects _FIFO2INT1 |
| | | | 0 | FIFO1SEL Select line for FIFO1INT [1..0] 0 = Selects _FIFO1INT0 1 = Selects _FIFO1INT1 |
| 08h | W | | 0 | CLR/_CLR, System Clear Control Register 0 = Clears system CLR 1 = Sets system CLR |
| A8h | W | | 15..0 | PCM TESTDATA [15..0], Test data value sent out to PCM generator in place of real data if PCMSEL = 1 |
| C8h | W | | 15..12 | DECOFF [3..0], See Channel 1 Address Map |
| | | | 11..8 | DECSEL [3..0], See Channel 1 Address Map |
| | | | 7 | SYNCCLK, See Channel 1 Address Map |
| | | | 6..4 | OUT_DEC [2..0], See Channel 1 Address Map |
| | | | 3 | Mode of operation, See Channel 1 Address Map |
| | | | 2..1 | DEVSEL [1..0], See Channel 1 Address Map |
| | | | 0 | CLKSEL, Selects A/D clock 0 = 15 MHz A/D clock 1 = 58.59375 kHz A/D clock |
| D0h | W | | 14 | _LDACOUT, See Channel 1 Address Map |
| | | | 12 | TSCOUTEN, See Channel 1 Address Map |
| | | | 11 | RECFIL, See Channel 1 Address Map |
| | | | 10..9 | AASEL [1..0], Selects the Anti-Alias Filter Setting 01 = Selects subcarrier upper band edge from 14648.4375 Hz to 3.5 MHz 10 = Selects subcarrier upper band edge from 250 Hz to 14648.4375 Hz 00, 11 = invalid |
| | | | 8..7 | INSEL [1..0], Selects between Analog Input 1 and 2 01 = Selects ANALOG1IN 10 = Selects ANALOG2IN 00, 11 = invalid |
| | | | 6..5 | FILSEL [1..0], See Channel 1 Address Map |
| | | | 4..2 | RECON [2..0], See Channel 1 Address Map |
| | | | 0 | OUTDACA/B, See Channel 1 Address Map |

System Address Map (cont.)

| Reg | R/W | Ch | Bits | Description |
|------|-----|----|--------|---|
| 100h | W | | 12 | DEMODREN, Demod Read Enable 0 = Enables LOCK [11..0] and DMLOCK readback at ODATA 1 = Enables DEMOD [15..0] readback at ODATA |
| | | | 11 | LOCKREN, Enables (LOCK [11..0] and DMLOCK) readback 0 = Enables the reading of the AGC OFFSET/GAIN value 1 = Enables read of LOCK [11..0] and DMLOCK [12] only if DEMODREN is 0 |
| | | | 10 | AGCOFF/GAINSEL, Enables AGC offset or gain values to be readback 0 = Enables OFF[7..0] for readback at ODATA 1 = Enables GAIN[7..0] for readback at ODATA |
| | | | 8 | PCMCLKPOL, Selects PCM 0° or 180° CLK polarity 0 = selects PCM 0° clock 0 = selects PCM 180° clock |
| | | | 7 | PCMCTCLR, Enables the clearing of the internal PCM addressing counter 0 = Disables the clear for the internal PCM address counter 1 = Sets the clear for the internal PCM address counter |
| | | | 6 | RNRZ-LSEL, Selection of NRZ-L or randomized NRZ-L PCM output 0 = Selects NRZ-L output PCM data format 1 = Selects randomized NRZ-L output PCM data format |
| | | | 5 | PN24SEL, Selects normal demodulator output or a Pseudo-random 24 pattern for bit sync checkout 0 = Selects normal demod output 1 = Selects Pseudo-Randomized 24 output from the demod output conn |
| | | | 4..0 | PCMOUTPUTCLOCK [4..0], Selection of PCM output clock rate as binary divisions of 60 MHz clock rate. Valid selections are 2 ¹ and 2 ¹⁷ (30 MHz to 457.7 Hz). |
| 110h | W | | 11 | PCMRAMSEL, Selection of RAM addressing for PCM RAM 0 = Selects loading the RAM with addressing from the VMEbus 1 = Selects loading the RAM with incremental addressing using an internal counter |
| | | | 10..0 | RAMADDR [10..0], RAM address bus when writing/reading RAM from VMEbus |
| 130h | W | | 15..12 | PCMASTER [3..0], Enter the address for the output PCM Generator board. This address matches the DIP SWITCH setting for SW1. |
| | | | 10..0 | FRAMECOUNT [10..0], The number of words in a PCM frame. |
| 418h | R | | | ODATA, Output data register (multipurpose) LOCK [11..0] and DMLOCK [12] See Channel 1 Address Map AGC Gain DAC (DACA) [7..0] if LOCKREN and DEMODREN = 0 and DACREN=0 AGC Offset DAC (DACB) [7..0] if LOCKREN and DEMODREN = 0 and DACREN=1 DEMOM [15..0] See Channel 1 Address Map |
| | | | 11..0 | LOCK [11..0], See Channel 1 Address Map |
| | | | 12 | DMLOCK [12], See Channel 1 Address Map |
| | | | 7..0 | DACA [7..0], Value of AGC Gain DAC |
| | | | 7..0 | DACB [7..0], Value of AGC Offset DAC |
| | | | 15..0 | DEMOM [15..0], See Channel 1 Address Map |
| 780h | R | | 7..0 | ASCII signature readback character "S" (01010011) |
| 788h | R | | 7..0 | ASCII signature readback character "Y" (01011001) |
| 790h | R | | 7..0 | ASCII signature readback character "D" (01000100) |
| 798h | R | | 7..0 | ASCII signature readback character "U" (01010101) |
| 7A0h | R | | 7..0 | ASCII signature readback character "A" (01000001) |
| 7A8h | R | | 7..0 | ASCII signature readback character "L" (01001100) |
| 7B0h | R | | 7..0 | ASCII signature readback character "1" (00110001) |
| 7B8h | R | | 7..0 | ASCII signature readback character "NULL" (00000000) |

System Address Map (cont.)

| Reg | R/W | Ch | Bits | Description |
|------|-----|----|--|---|
| 528h | W | | 15..8 | IAGC SD [7..0], AGC DAC Control |
| | | | 7..6 | AD SPEED, Clock Speed for AGC control from 0.1 to 10 msec |
| | | | 5 | _IAGC CS, AGC DAC chip select (active low) |
| | | | 4 | _IAGC LD, AGC Load (active low) |
| | | | 3 | _IAGC WR, AGC Write (active low) |
| | | | 2 | _IAGC CLR, AGC Clear (active low) |
| | | | 1 | _IAGC A/B, Select DAC A or DAC B 0 = Select DAC A 1 = Select DAC B |
| | | 0 | AUTO AGC, Control line used to select manual or auto for AGC control lines (IAGCSD [7..0], _IAGCCS, _IAGCLD, _IAGCWR, and IAGCA/B). 0 = FACTORY TEST CONTROL REGISTER Selects manual loading of AGC over the VMEbus. 1 = Selects auto loading of the AGC Control lines. In auto mode the AGC uses a decode and state machine format to control the AGC. | |
| 98h | W | | 11..8 | MUXSEL [3..0], See Channel 1 Address Map |
| | | | 3 | PCMSSEL, Selects between data and an internal test value 0 = Real data 1 = Test data |
| | | | 2 | MODOUT, See Channel 1 Address Map |
| | | | 1 | RD SEL, Selects between TSC [11..0] or CONF_DONE [11..0] to be read 0 = Enables CONF_DONE [11..0] to be read 1 = Enables TSC [11..0] to be read |
| | | | 0 | DEV CLR, See Channel 1 Address Map |
| A0h | R | | 11..0 | TSC/CONF_DONE (selected by Reg 98h bit 1) If TSC [11..0], Driven by a demodulator used as a reference channel and multiplied by DEV_CNST [15..0] for Tape Speed Compensation input to data channels. If CONF_DONE [11..0], Altera configuration done bit for 11 Alteras. CONF_DONE [0] = U23, Channel 1 CONF_DONE [1] = U7, Channel 1 CONF_DONE [2] = U20, Channel 1 CONF_DONE [3] = U1, Channel 1 CONF_DONE [4] = U10, Channel 1 CONF_DONE [5] = U42, Channel 2 CONF_DONE [6] = U60, Channel 2 CONF_DONE [7] = U49, Channel 2 CONF_DONE [8] = U66, Channel 2 CONF_DONE [9] = U52, Channel 2 CONF_DONE [10] = U30, Channel 1 |
| 498h | W | | 11..8 | MUXSEL [3..0], See Channel 2 Address Map |
| | | | 3 | PCMSSEL, Selects between data and an internal test value 0 = Real data 1 = Test data |
| | | | 2 | MODOUT, See Channel 2 Address Map |
| | | | | |
| | | | 0 | DEV CLR, See Channel 2 Address Map |

System Address Map (cont.)

| Reg | R/W | Ch | Bits | Description |
|------|-----|----|-------|---|
| 120h | W | | 15..0 | RAMIDATA [15..0], Data stored in RAM of PCM generator corresponding to BD address to be enabled for PCM output. |
| 500h | W | | 12 | DEMODREN, Demod Read Enable 0 = Enables LOCK [11..0] and DMLOCK readback at ODATA 1 = Enables DEMOD [15..0] readback at ODATA |
| | | | 11 | LOCKREN, Enables (LOCK [11..0] and DMLOCK) readback 0 = Enables the reading of the AGC OFFSET/GAIN value 1 = Enables read of LOCK [11..0] and DMLOCK [12] only if DEMODREN is 0 |
| | | | 10 | AGCOFF/GAINSEL, Enables AGC offset or gain values to be readback 0 = Enables OFF[7..0] for readback at ODATA 1 = Enables GAIN[7..0] for readback at ODATA |
| | | | 7 | PCMCTCLR, Enables the clearing of the internal PCM addressing counter 0 = Disables the clear for the internal PCM address counter 1 = Sets the clear for the internal PCM address counter |
| | | | 6 | RNRZ-LSEL, Selection of NRZ-L or randomized NRZ-L PCM output 0 = Selects NRZ-L output PCM data format 1 = Selects randomized NRZ-L output PCM data format |
| | | | 5 | PN24SEL, Selects normal demodulator output or a Pseudo-random 24 pattern for bit sync checkout 0 = Selects normal demod output 1 = Selects Pseudo-Randomized 24 output from the demod output conn |
| | | | 4..0 | PCMOUTPUTCLOCK [4..0], Selection of PCM output clock rate as binary divisions of 60 MHz clock rate. Valid selections are 2^1 and 2^{17} (30 MHz to 457.7 Hz). |

4.2 Channel 1 Address Map

| Reg | R/W | Ch | Bits | Description |
|-----|-----|----|--------|--|
| 40h | W | 1 | 7..0 | RECON BSD [7..0], 8 bit unsigned short form from 0x0000 to 0x00ff to control Reconstruction Filter fine tune DAC. |
| 48h | W | 1 | 7..0 | OUTPUT BSD [7..0], 8 bit unsigned short form from 0x0000 to 0x00ff to control Analog Output Gain/Offset DAC. |
| 80h | W | 1 | 15..0 | PHASE STEP [31..16], NCO Phase Accumulator Step size |
| 88h | W | 1 | 15..0 | PHASE STEP [15..0], NCO Phase Accumulator Step size |
| 90h | W | 1 | 15..0 | DEV_CNST [15..0], Downconverter Deviation Multiplication factor |
| 98h | W | 1 | 11..8 | MUXSEL [3..0], Number of decimations for mux decimation filter from 0 to 8 |
| | | | 3 | PCMSEL, See System Address Map |
| | | | 2 | MODOUT, Selects between MNCO function as downconverter or modulator 0 = Downconverted (using DOWN [11..0]) 1 = SIN/COS multiplied by 0x7ff constant (no downconversion) INVALID, Factory Test Control Register. |
| | | | 1 | RD SEL, See System Address Map |
| | | | 0 | DEV CLR, Used to enable or clear the frequency deviation input register 0 = Enables frequency deviation input data register 1 = Clears frequency deviation input data register |
| C0h | W | 1 | 15..0 | DEV [15..0], Deviation multiplication factor for output scaling (WRITE) |
| C8h | W | 1 | 15..12 | DECOFF [3..0], Decimation offset selection summed with SIN/COS [11..0] |
| | | | 11..8 | DECSEL [3..0], Number of SIN/COS decimations from 0 to 8 |
| | | | 7 | SYNCLK, Data clock synchronization 0 = Deselects data clock synchronization 1 = Selects data clock synchronization |
| | | | 6..4 | OUT_DEC [2..0], Number of Output decimations from 0 to 6 |
| | | | 3 | Mode of operation 0 = FM mode (ARCTAN data) 1 = INVALID |
| | | | 2..1 | DEVSEL [1..0], Deviation Pipeline multiplication scale factor from 0 to 3 |
| | | | 0 | CLKSEL, See System Address Map |
| D0h | W | 1 | 14 | _LDACOUT, Load pulse 0 = Enables the load pulse for the output gain/offset DAC 1 = removes the load pulse from the output gain/offset DAC |
| | | | 12 | TSCOUTEN, Tape Speed Compensation Enable 0 = no effect 1 = enables the channel to be used as a REF channel allowing it's DEMOD [11..0] bus to drive other channels for TSC |
| | | | 11 | RECFIL, Analog Reconstruction Filter enable 0 = Demod DAC output data bypasses (skips) the analog reconstruction filter. 1 = Demod DAC output data uses the analog reconstruction filter. |
| | | | 10..9 | AASEL [1..0], See System Address Map |
| | | | 8..7 | INSEL [1..0], See System Address Map |
| | | | 6..5 | FILSEL [1..0], Deviation Coefficient (ROM-fine selection) filter selection |
| | | | 4..2 | RECON [2..0], Analog Reconstruction Filter range selection 000 = OutputFilterFrequency Frequencies from 45 kHz to 1 MHz 001 = OutputFilterFrequency Frequencies from 4 kHz to 45 kHz 011 = OutputFilterFrequency Frequencies from 400 Hz to 4 kHz 111 = OutputFilterFrequency Frequencies from 1 Hz to 400 Hz All other bit selections are invalid. |
| | | | 0 | OUTDACA/B, Selects Output DAC (gain or offset) 0 = Gain DAC A is active 1 = Offset DAC B is active |

Channel 1 Address Map (cont.)

| Reg | R/W | Ch | Bits | Description |
|------|-----|----|-------|---|
| D8h | R | 1 | 15..0 | DEV [15..0], Deviation multiplication factor for output scaling (READ) |
| E0h | W | 1 | 3..0 | FCLKSEL [3..0], SIN/COS decimation FCLK output selection |
| 140h | W | 1 | 4 | SELINT, Selects FIFO interrupt conditions 0 = Selects FIFOPAE (partially empty) as FIFOINT0 and FIFOPAF (partially full) as FIFOINT1 1 = Selects FIFOOEF (empty) as FIFOINT0 and FIFOOFF (full) as FIFOINT1 |
| | | | 3 | _FIFOREN/_FIFOOE, FIFO read enable 0 = Enables FIFO to be read 1 = Disables FIFO read |
| | | | 2 | _FIFOLD, FIFO load enable 0 = Enables FIFO load 1 = Disables FIFO load |
| | | | 1 | _FIFORST, FIFO reset enable 0 = Enables FIFO reset 1 = Disables FIFO reset |
| | | | 0 | OUTMUXSEL, Selects source of data to FIFOIN [15..0] 0 = Selects DEMOD [15..0] data as source of data to FIFOIN 1 = Selects FDATA [15..0] data (internal)as source of data to FIFOIN |
| 148h | R | 1 | 15..0 | FIFO [15..0], FIFO data |
| 160h | W | 1 | 15..0 | FDATA [15..0], Registered data for debug purposes |
| 168h | R | 1 | 3 | _FIFOFF, FIFO full flag 0 = FIFO full 1 = FIFO not full |
| | | | 2 | _FIFPAF, FIFO partially full flag 0 = FIFO partially full 1 = FIFO not partially full |
| | | | 1 | _FIFOOEF, FIFO empty flag 0 = FIFO empty 1 = FIFO not empty |
| | | | 0 | _FIFPAE, FIFO partially empty flag 0 = FIFO partially empty 1 = FIFO not partially empty |
| 200h | W | 1 | 11..0 | RAMCOEFF0, Output FIR filter coefficient 0 |
| 208h | W | 1 | 11..0 | RAMCOEFF1, Output FIR filter coefficient 1 |
| 210h | W | 1 | 11..0 | RAMCOEFF2, Output FIR filter coefficient 2 |
| 218h | W | 1 | 11..0 | RAMCOEFF3, Output FIR filter coefficient 3 |
| 220h | W | 1 | 11..0 | RAMCOEFF4, Output FIR filter coefficient 4 |
| 228h | W | 1 | 11..0 | RAMCOEFF5, Output FIR filter coefficient 5 |
| 230h | W | 1 | 11..0 | RAMCOEFF6, Output FIR filter coefficient 6 |
| 238h | W | 1 | 11..0 | RAMCOEFF7, Output FIR filter coefficient 7 |
| 240h | W | 1 | 11..0 | RAMCOEFF8, Output FIR filter coefficient 8 |
| 248h | W | 1 | 11..0 | RAMCOEFF9, Output FIR filter coefficient 9 |
| 250h | W | 1 | 11..0 | RAMCOEFF10, Output FIR filter coefficient 10 |
| 258h | W | 1 | 11..0 | RAMCOEFF11, Output FIR filter coefficient 11 |
| 260h | W | 1 | 11..0 | RAMCOEFF12, Output FIR filter coefficient 12 |
| 268h | W | 1 | 11..0 | RAMCOEFF13, Output FIR filter coefficient 13 |
| 270h | W | 1 | 11..0 | RAMCOEFF14, Output FIR filter coefficient 14 |
| 278h | W | 1 | 11..0 | RAMCOEFF15, Output FIR filter coefficient 15 |

Channel 1 Address Map (cont.)

| Reg | R/W | Ch | Bits | Description |
|------|-----|----|-------|---|
| 280h | R | 1 | 11..0 | RAMCOEFF0, Output FIR filter coefficient 0 |
| 288h | R | 1 | 11..0 | RAMCOEFF1, Output FIR filter coefficient 1 |
| 290h | R | 1 | 11..0 | RAMCOEFF2, Output FIR filter coefficient 2 |
| 298h | R | 1 | 11..0 | RAMCOEFF3, Output FIR filter coefficient 3 |
| 2A0h | R | 1 | 11..0 | RAMCOEFF4, Output FIR filter coefficient 4 |
| 2A8h | R | 1 | 11..0 | RAMCOEFF5, Output FIR filter coefficient 5 |
| 2B0h | R | 1 | 11..0 | RAMCOEFF6, Output FIR filter coefficient 6 |
| 2B8h | R | 1 | 11..0 | RAMCOEFF7, Output FIR filter coefficient 7 |
| 2C0h | R | 1 | 11..0 | RAMCOEFF8, Output FIR filter coefficient 8 |
| 2C8h | R | 1 | 11..0 | RAMCOEFF9, Output FIR filter coefficient 9 |
| 2D0h | R | 1 | 11..0 | RAMCOEFF10, Output FIR filter coefficient 10 |
| 2D8h | R | 1 | 11..0 | RAMCOEFF11, Output FIR filter coefficient 11 |
| 2E0h | R | 1 | 11..0 | RAMCOEFF12, Output FIR filter coefficient 12 |
| 2E8h | R | 1 | 11..0 | RAMCOEFF13, Output FIR filter coefficient 13 |
| 2F0h | R | 1 | 11..0 | RAMCOEFF14, Output FIR filter coefficient 14 |
| 2F8h | R | 1 | 11..0 | RAMCOEFF15, Output FIR filter coefficient 15 |
| 300h | R | 1 | 15..0 | OUTFIL [15..0], 32 Tap FIR OutputFilterFrequency Output Data |
| 308h | W | 1 | 1 | OUTSEL, Selects the use or bypass of the 32 Tap FIR OutputFilterFrequency 0 = Enables the use of the 32 Tap FIR Filter (Normal Mode) 1 = Bypasses (disables) the 32 Tap FIR Filter |
| | | | 0 | RAMSEL, RAM Address selection for 32 Tap FIR OutputFilterFrequency 0 = Selects addressing the FIR coefficients using VME addressing 1 = Selects addressing the FIR coefficients using internal addressing |
| 100h | W | 1 | 12 | DEMODREN, See System Address Map |
| | | | 11 | LOCKREN, See System Address Map |
| | | | 10 | AGCOFF/GAINSEL, See System Address Map |
| | | | 7 | PCMCTCLR, See System Address Map |
| | | | 6 | RNRZ-LSEL, See System Address Map |
| | | | 5 | PN24SEL, See System Address Map |
| | | | 4..0 | PCMOUTPUTCLOCK [4..0], See System Address Map |
| 108h | W | 1 | 11..0 | LOCKREG [11..0], Value that LOCK [11..0] must be greater than to enable DMLOCK (lock indicator) |
| 118h | R | 1 | | ODATA, Output data register (multipurpose) LOCK [11..0] and DMLOCK [12] if DEMODREN = 0 and LOCKREN = 1 DEMOD [15..0] if DEMODREN = 1 |
| | | | 11..0 | LOCK [11..0], Sum of 8 samples of SINDEC [11..0] data to detect "inband" energy to compare to LOCKREG [11..0] to determine lock status (DMLOCK) |
| | | | 12 | DMLOCK [12], Demod Lock Status, 1 = lock, 0 = no lock |
| | | | | |
| | | | 15..0 | DEMOD [15..0], FACTORY TEST CONTROL REGISTER Value of demodulated data in offset binary format. |

4.3 Channel 2 Address Map

| Reg | R/W | Ch | Bits | Description |
|------|-----|----|--------|--|
| 440h | W | 1 | 7..0 | RECON BSD [7..0], 8 bit unsigned short form from 0x0000 to 0x00ff to control Reconstruction Filter fine tune DAC. |
| 448h | W | 1 | 7..0 | OUTPUT BSD [7..0], 8 bit unsigned short form from 0x0000 to 0x00ff to control Analog Output Gain/Offset DAC. |
| 480h | W | 1 | 15..0 | PHASE STEP [31..16], NCO Phase Accumulator Step size |
| 488h | W | 1 | 15..0 | PHASE STEP [15..0], NCO Phase Accumulator Step size |
| 490h | W | 1 | 15..0 | DEV_CNST [15..0], Downconverter Deviation Multiplication factor |
| 498h | W | 1 | 11..8 | MUXSEL [3..0], Number of decimations for mux decimation filter from 0 to 8 |
| | | | 3 | PCMSEL, See System Address Map |
| | | | 2 | MODOUT, Selects between MNCO function as downconverter or modulator 0 = Downconverted (using DOWN [11..0]) 1 = SIN/COS multiplied by 0x7ff constant (no downconversion) |
| | | | 0 | DEV CLR, Used to enable or clear the frequency deviation input register 0 = Enables frequency deviation input data register 1 = Clears frequency deviation input data register |
| 4C0h | W | 1 | 15..0 | DEV [15..0], Deviation multiplication factor for output scaling (WRITE) |
| 4C8h | W | 1 | 15..12 | DECOFF [3..0], Decimation offset selection summed with SIN/COS [11..0] |
| | | | 11..8 | DECSEL [3..0], Number of SIN/COS decimations from 0 to 8 |
| | | | 7 | SYNCLK, Data clock synchronization 0 = Deselects data clock synchronization 1 = Selects data clock synchronization |
| | | | 6..4 | OUT_DEC [2..0], Number of Output decimations from 0 to 6 |
| | | | 3 | Mode of operation 0 = FM mode (ARCTAN data) 1 = INVALID |
| | | | 2..1 | DEVSEL [1..0], Deviation Pipeline multiplication scale factor from 0 to 3 |
| 4D0h | W | 1 | 14 | _LDACOUT, Load pulse 0 = Enables the load pulse for the output gain/offset DAC 1 = removes the load pulse from the output gain/offset DAC |
| | | | 12 | TSCOUTEN, Tape Speed Compensation Enable 0 = no effect 1 = enables the channel to be used as a REF channel allowing it's DEMOD [11..0] bus to drive other channels for TSC |
| | | | 11 | RECFIL, Analog Reconstruction Filter enable 0 = Demod DAC output data bypasses (skips) the analog reconstruction filter. 1 = Demod DAC output data uses the analog reconstruction filter. |
| | | | | |
| | | | | |
| | | | 6..5 | FILSEL [1..0], Deviation Coefficient (ROM-fine selection) filter selection |
| | | | 4..2 | RECON [2..0], Analog Reconstruction Filter range selection 000 = OutputFilterFrequency Frequencies from 45 kHz to 1 MHz 001 = OutputFilterFrequency Frequencies from 4 kHz to 45 kHz 011 = OutputFilterFrequency Frequencies from 400 Hz to 4 kHz 111 = OutputFilterFrequency Frequencies from 1 Hz to 400 Hz All other bit selections are invalid. |
| | | | 0 | OUTDACA/B, Selects Output DAC (gain or offset) 0 = Gain DAC A is active 1 = Offset DAC B is active |

Channel 2 Address Map (cont.)

| Reg | R/W | Ch | Bits | Description |
|------|-----|----|-------|---|
| 4D8h | R | 1 | 15..0 | DEV [15..0], Deviation multiplication factor for output scaling (READ) |
| 4E0h | W | 1 | 3..0 | FCLKSEL [3..0], SIN/COS decimation FCLK output selection |
| 540h | W | 1 | 4 | SELINT, Selects FIFO interrupt conditions 0 = Selects FIFOPAE (partially empty) as FIFOINT0 and FIFOPAF (partially full) as FIFOINT1 1 = Selects FIFOOEF (empty) as FIFOINT0 and FIFOOFF (full) as FIFOINT1 |
| | | | 3 | _FIFOREN/_FIFOOE, FIFO read enable 0 = Enables FIFO to be read 1 = Disables FIFO read |
| | | | 2 | _FIFOLD, FIFO load enable 0 = Enables FIFO load 1 = Disables FIFO load |
| | | | 1 | _FIFORST, FIFO reset enable 0 = Enables FIFO reset 1 = Disables FIFO reset |
| | | | 0 | OUTMUXSEL, Selects source of data to FIFOIN [15..0] 0 = Selects DEMOD [15..0] data as source of data to FIFOIN 1 = Selects FDATA [15..0] data (internal) as source of data to FIFOIN |
| 548h | R | 1 | 15..0 | FIFO [15..0], FIFO data |
| 560h | W | 1 | 15..0 | FDATA [15..0], Registered data for debug purposes |
| 568h | R | 1 | 3 | _FIFOFF, FIFO full flag 0 = FIFO full 1 = FIFO not full |
| | | | 2 | _FIFPAF, FIFO partially full flag 0 = FIFO partially full 1 = FIFO not partially full |
| | | | 1 | _FIFOOEF, FIFO empty flag 0 = FIFO empty 1 = FIFO not empty |
| | | | 0 | _FIFPAE, FIFO partially empty flag 0 = FIFO partially empty 1 = FIFO not partially empty |
| 600h | W | 1 | 11..0 | RAMCOEFF0, Output FIR filter coefficient 0 |
| 608h | W | 1 | 11..0 | RAMCOEFF1, Output FIR filter coefficient 1 |
| 610h | W | 1 | 11..0 | RAMCOEFF2, Output FIR filter coefficient 2 |
| 618h | W | 1 | 11..0 | RAMCOEFF3, Output FIR filter coefficient 3 |
| 620h | W | 1 | 11..0 | RAMCOEFF4, Output FIR filter coefficient 4 |
| 628h | W | 1 | 11..0 | RAMCOEFF5, Output FIR filter coefficient 5 |
| 630h | W | 1 | 11..0 | RAMCOEFF6, Output FIR filter coefficient 6 |
| 638h | W | 1 | 11..0 | RAMCOEFF7, Output FIR filter coefficient 7 |
| 640h | W | 1 | 11..0 | RAMCOEFF8, Output FIR filter coefficient 8 |
| 648h | W | 1 | 11..0 | RAMCOEFF9, Output FIR filter coefficient 9 |
| 650h | W | 1 | 11..0 | RAMCOEFF10, Output FIR filter coefficient 10 |
| 658h | W | 1 | 11..0 | RAMCOEFF11, Output FIR filter coefficient 11 |
| 660h | W | 1 | 11..0 | RAMCOEFF12, Output FIR filter coefficient 12 |
| 668h | W | 1 | 11..0 | RAMCOEFF13, Output FIR filter coefficient 13 |
| 670h | W | 1 | 11..0 | RAMCOEFF14, Output FIR filter coefficient 14 |
| 678h | W | 1 | 11..0 | RAMCOEFF15, Output FIR filter coefficient 15 |

Channel 2 Address Map (cont.)

| Reg | R/W | Ch | Bits | Description |
|------|-----|----|-------|---|
| 680h | R | 1 | 11..0 | RAMCOEFF0, Output FIR filter coefficient 0 |
| 688h | R | 1 | 11..0 | RAMCOEFF1, Output FIR filter coefficient 1 |
| 690h | R | 1 | 11..0 | RAMCOEFF2, Output FIR filter coefficient 2 |
| 698h | R | 1 | 11..0 | RAMCOEFF3, Output FIR filter coefficient 3 |
| 6A0h | R | 1 | 11..0 | RAMCOEFF4, Output FIR filter coefficient 4 |
| 6A8h | R | 1 | 11..0 | RAMCOEFF5, Output FIR filter coefficient 5 |
| 6B0h | R | 1 | 11..0 | RAMCOEFF6, Output FIR filter coefficient 6 |
| 6B8h | R | 1 | 11..0 | RAMCOEFF7, Output FIR filter coefficient 7 |
| 6C0h | R | 1 | 11..0 | RAMCOEFF8, Output FIR filter coefficient 8 |
| 6C8h | R | 1 | 11..0 | RAMCOEFF9, Output FIR filter coefficient 9 |
| 6D0h | R | 1 | 11..0 | RAMCOEFF10, Output FIR filter coefficient 10 |
| 6D8h | R | 1 | 11..0 | RAMCOEFF11, Output FIR filter coefficient 11 |
| 6E0h | R | 1 | 11..0 | RAMCOEFF12, Output FIR filter coefficient 12 |
| 6E8h | R | 1 | 11..0 | RAMCOEFF13, Output FIR filter coefficient 13 |
| 6F0h | R | 1 | 11..0 | RAMCOEFF14, Output FIR filter coefficient 14 |
| 6F8h | R | 1 | 11..0 | RAMCOEFF15, Output FIR filter coefficient 15 |
| 700h | R | 2 | 15..0 | OUTFIL [15..0], 32 Tap FIR OutputFilterFrequency Output Data |
| 708h | W | 2 | 1 | OUTSEL, Selects the use or bypass of the 32 Tap FIR OutputFilterFrequency 0 = Enables the use of the 32 Tap FIR Filter (Normal Mode) 1 = Bypasses (disables) the 32 Tap FIR Filter |
| | | | 0 | RAMSEL, RAM Address selection for 32 Tap FIR OutputFilterFrequency 0 = Selects loading the RAM coefficients with address control over the VMEbus 1 = Selects loading the RAM coefficients using incremental addressing by internal counter |
| 500h | W | 2 | 12 | DEMODREN, Demod Read Enable 0 = Enables LOCK [11..0] and DMLOCK or AGC DAC readback at ODATA 1 = Enables DEMOD [15..0] readback at ODATA |
| | | | 11 | LOCKREN, Enables (LOCK [11..0] and DMLOCK) or AGC DAC readback 0 = Enables AGC DAC read only if DEMODREN is 0 1 = Enables read of LOCK [11..0] and DMLOCK [12] only if DEMODREN is 0 |
| | | | 10 | DACREN, Selects read of AGC Gain or Offset DAC 0 = Enables read of AGC Gain DAC (DAC A) if LOCKREN and DEMODREN= 0 1 = Enables read of AGC Offset DAC (DAC B) if LOCKREN and DEMODREN=0 |
| | | | | |
| 508h | W | 2 | 11..0 | LOCKREG [11..0], Value that LOCK [11..0] must be greater than to enable DMLOCK (lock indicator) |
| 518h | R | 2 | | ODATA, Output data register (multipurpose) LOCK [11..0] and DMLOCK [12] if DEMODREN = 0 and LOCKREN = 1 AGC Gain DAC (DACA) [7..0] See System Address Map AGC Offset DAC (DACB) [7..0] See System Address Map DEMOD [15..0] if DEMODREN = 1 |
| | | | 11..0 | LOCK [11..0], Sum of 8 samples of SINDEC [11..0] data to detect "inband" energy to compare to LOCKREG [11..0] to determine lock status (DMLOCK) |
| | | | 12 | DMLOCK [12], Demod Lock Status, 1 = lock, 0 = no lock |
| | | 2 | 7..0 | DACA [7..0], See System Address Map |
| | | 2 | 7..0 | DACB [7..0], See System Address Map |
| | | | 15..0 | DEMOD [15..0], FACTORY TEST CONTROL REGISTER Value of demodulated data in offset binary format. |
| | | | | |

Chapter 5 Example Frequency Register Writes

This chapter has example register address download values for some standard frequencies. Hopefully, these examples will help guide the programmer in verifying the address map. The order of the write sequences must be followed as shown in the following tables.

5.1 Input 1, Output 1 - 64 kHz Center Frequency, 4 kHz Deviation, 2 kHz Output Filter Frequency, Analog Output Filter Mode, Analog Output Level 5.0 Vpp, Analog Output Offset 0.0 VDC

| Demod Channel Number | VME ADDR | 16 Bit Data Value | Description |
|----------------------|----------|-------------------|---|
| System | 08h | 0001h | System clear all control registers |
| System | 08h | 0000h | Disable system clear all control registers |
| System | 100h | 0000h | Enable Demod Output from OUT1 |
| System | 528h | 0041h | AGC enable |
| System & 1 | D0h | 4aach | AASEL, INSEL, FILSEL, RECON, analog recon enabled |
| 1 | 98h | 0500h | MUXDEC – Multiplex Decimations |
| 1 | 80h | 22f3h | PHASESTEP[31..16] |
| 1 | 88h | d939h | PHASESTEP[15..0] |
| 1 | C8h | 5414h | DECOFF, DECSEL, OUTDEC, DEVSEL, CLKSEL |
| 1 | E0h | 8h | FCLKSEL |
| 1 | C0h | 9c8dh | DEVSCALAR[15..0] – Deviation Scalar |
| 1 | 308h | 0h | Enable VME coef addressing |
| 1 | 200h | fffh | Tblidx = 3, acoef 0 |
| 1 | 208h | ffch | Tblidx = 3, acoef 1 |
| 1 | 210h | fffh | Tblidx = 3, acoef 2 |
| 1 | 218h | 00bh | Tblidx = 3, acoef 3 |
| 1 | 220h | 011h | Tblidx = 3, acoef 4 |
| 1 | 228h | ffbh | Tblidx = 3, acoef 5 |
| 1 | 230h | fd5h | Tblidx = 3, acoef 6 |
| 1 | 238h | fdbh | Tblidx = 3, acoef 7 |
| 1 | 240h | 02dh | Tblidx = 3, acoef 8 |
| 1 | 248h | 077h | Tblidx = 3, acoef 9 |
| 1 | 250h | 028h | Tblidx = 3, acoef 10 |
| 1 | 258h | f49h | Tblidx = 3, acoef 11 |
| 1 | 260h | ef0h | Tblidx = 3, acoef 12 |
| 1 | 268h | 055h | Tblidx = 3, acoef 13 |
| 1 | 270h | 33ah | Tblidx = 3, acoef 14 |
| 1 | 278h | 5abh | Tblidx = 3, acoef 15 |
| 1 | 308h | 0001h | Enable internal coef addressing, OUTSEL |
| 1 | 40h | 00B9h | RECONBSD - Reconstruction filter fine |
| 1 | D0h | 4aadh | OUTDAC A/B = 1 - Select output offset DAC |
| 1 | 48h | 80h | AOUTPUT - Analog offset value |
| 1 | D0h | 0aadh | Drop _LDACOUT to load DAC |
| 1 | D0h | 4aadh | Clear _LDACOUT to complete load of DAC |
| 1 | D0h | 4aach | OUTDAC A/B = 0 - Select output gain DAC |
| 1 | 48h | 00C3h | AGAIN - Set analog output gain |
| 1 | D0h | 0aach | Drop _LDACOUT to load DAC |
| 1 | D0h | 4aach | Clear _LDACOUT to complete load of DAC |
| 1 | 108h | 0030h | Demod lock compare value |

5.2 Input 1, Output 1 – 1.8 MHz Center Frequency, 720 kHz Deviation, 720 kHz Output Filter Frequency, Digital Output Filter Mode, Analog Output Level 10.0 Vpp, Analog Output Offset 0.0 VDC

| Demod Channel Number | VME ADDR | 16 Bit Data Value | Description |
|-----------------------------|-----------------|--------------------------|---|
| System | 08h | 0001h | System clear all control registers |
| System | 08h | 0000h | Disable system clear all control registers |
| System | 100h | 0000h | Enable Demod Output from OUT1 |
| System | 528h | 0041h | AGC enable |
| System & 1 | D0h | 4ae0h | AASEL, INSEL, FILSEL, RECON, analog recon enabled |
| 1 | 98h | 0000h | MUXDEC – Multiplex Decimations |
| 1 | 80h | 1eb8h | PHASESTEP[31..16] |
| 1 | 88h | 51ech | PHASESTEP[15..0] |
| 1 | C8h | 3204h | DECOFF, DECSEL, OUTDEC, DEVSEL, CLKSEL |
| 1 | E0h | 1h | FCLKSEL |
| 1 | C0h | B948h | DEVSCALAR[15..0] – Deviation Scalar |
| 1 | 308h | 0h | Enable VME coef addressing |
| 1 | 200h | 000h | Tblidx = 9, dcoef 0 |
| 1 | 208h | 002h | Tblidx = 9, dcoef 1 |
| 1 | 210h | 005h | Tblidx = 9, dcoef 2 |
| 1 | 218h | 000h | Tblidx = 9, dcoef 3 |
| 1 | 220h | ffch | Tblidx = 9, dcoef 4 |
| 1 | 228h | 00fh | Tblidx = 9, dcoef 5 |
| 1 | 230h | 006h | Tblidx = 9, dcoef 6 |
| 1 | 238h | fe8h | Tblidx = 9, dcoef 7 |
| 1 | 240h | 021h | Tblidx = 9, dcoef 8 |
| 1 | 248h | 021h | Tblidx = 9, dcoef 9 |
| 1 | 250h | fb9h | Tblidx = 9, dcoef 10 |
| 1 | 258h | 043h | Tblidx = 9, dcoef 11 |
| 1 | 260h | 07ch | Tblidx = 9, dcoef 12 |
| 1 | 268h | f3eh | Tblidx = 9, dcoef 13 |
| 1 | 270h | 14bh | Tblidx = 9, dcoef 14 |
| 1 | 278h | 6bdh | Tblidx = 9, dcoef 15 |
| 1 | 308h | 0001h | Enable internal coef addressing, OUTSEL |
| 1 | 40h | 00d9h | RECONBSD - Reconstruction filter fine |
| 1 | D0h | 4ae1h | OUTDAC A/B = 1 - Select output offset DAC |
| 1 | 48h | 80h | AOUTPUT - Analog offset value |
| 1 | D0h | 0ae1h | Drop _LDACOUT to load DAC |
| 1 | D0h | 4ae1h | Clear _LDACOUT to complete load of DAC |
| 1 | D0h | 4ae0h | OUTDAC A/B = 0 - Select output gain DAC |
| 1 | 48h | 00eeh | AGAIN - Set analog output gain |
| 1 | D0h | 0ae0h | Drop _LDACOUT to load DAC |
| 1 | D0h | 4ae0h | Clear _LDACOUT to complete load of DAC |
| 1 | 108h | 0030h | Demod lock compare value |

5.3 Input 1, Output 2 – 8 kHz Center Frequency, 2 kHz Deviation, 1 kHz Output Filter Frequency, Analog Output Filter Mode, Analog Output Level 10.0 Vpp, Analog Output Offset 0.0 VDC

| Demod Channel Number | VME ADDR | 16 Bit Data Value | Description |
|-----------------------------|-----------------|--------------------------|--|
| System | 08h | 0001h | System clear all control registers |
| System | 08h | 0000h | Disable system clear all control registers |
| System | 500h | 0000h | Enable Demod Output from OUT2 |
| System | 528h | 0041h | AGC enable |
| System | D0h | 4c80h | AASEL, INSEL |
| System | C8h | 0001h | CLKSEL |
| 2 | 498h | 0000h | MUXDEC – Multiplex Decimations |
| 2 | 480h | 22f3h | PHASESTEP[31..16] |
| 2 | 488h | D939h | PHASESTEP[15..0] |
| 2 | 4C8h | 3215h | DECOFF, DECSEL, OUTDEC, DEVSEL |
| 2 | 4E0h | 9h | FCLKSEL |
| 2 | 4C0h | 9c8dh | DEVSCALAR[15..0] – Deviation Scalar |
| 2 | 4d0h | 482ch | FILSEL, RECON |
| 2 | 708h | 0h | Enable VME coef addressing |
| 2 | 600h | fffh | Tblidx = 3, acoef 0 |
| 2 | 608h | ffch | Tblidx = 3, acoef 1 |
| 2 | 610h | fffh | Tblidx = 3, acoef 2 |
| 2 | 618h | 00bh | Tblidx = 3, acoef 3 |
| 2 | 620h | 011h | Tblidx = 3, acoef 4 |
| 2 | 628h | ffbh | Tblidx = 3, acoef 5 |
| 2 | 630h | fd5h | Tblidx = 3, acoef 6 |
| 2 | 638h | fdbh | Tblidx = 3, acoef 7 |
| 2 | 640h | 02dh | Tblidx = 3, acoef 8 |
| 2 | 648h | 077h | Tblidx = 3, acoef 9 |
| 2 | 650h | 028h | Tblidx = 3, acoef 10 |
| 2 | 658h | f49h | Tblidx = 3, acoef 11 |
| 2 | 660h | ef0h | Tblidx = 3, acoef 12 |
| 2 | 668h | 055h | Tblidx = 3, acoef 13 |
| 2 | 670h | 33ah | Tblidx = 3, acoef 14 |
| 2 | 678h | 5abh | Tblidx = 3, acoef 15 |
| 2 | 708h | 0001h | Enable internal coef addressing, OUTSEL |
| 2 | 440h | 0096h | RECONBSD - Reconstruction filter fine |
| 2 | 4D0h | 482dh | OUTDAC A/B = 1 - Select output offset DAC |
| 2 | 448h | 80h | AOUTPUT - Analog offset value |
| 2 | 4D0h | 082dh | Drop _LDACOUT to load DAC |
| 2 | 4D0h | 482dh | Clear _LDACOUT to complete load of DAC |
| 2 | 4D0h | 482ch | OUTDAC A/B = 0 - Select output gain DAC |
| 2 | 448h | 00eeh | AGAIN - Set analog output gain |
| 2 | 4D0h | 082ch | Drop _LDACOUT to load DAC |
| 2 | 4D0h | 482ch | Clear _LDACOUT to complete load of DAC |
| 2 | 508h | 0030h | Demod lock compare value |