ARCHI Series

Handheld Portable Complete Telemetry Standalone Processing Systems

ARCHI-PCM

ARCHI-RF

Introducing Ulyssix's portable telemetry processing products. The ARCHI-PCM system includes dual bit sync/frame sync/PCM decom, IRIG Time Code Reader, PCM simulator, and full feature PCM BERT.

The ARCHI-RF system includes all the ARCHI-PCM capabilities plus dual telemetry receivers with diversity combining and optional RF modulated signal generator capability to be a complete portable ground station including a full feature RF BERT.

The fully integrated ARCHI housing contains an embedded INTEL core processing single board computer, 1 TB SSHD, a 9.3" x 3.7", 1600 x 600 HDMI touchscreen/ display user interface for full user interaction for standalone system setup, display monitoring, and Ethernet interfacing.

All ARCHI systems display, analyze, archive, and/or Ethernet transport in either PCM UDP packets of either PCM frame or engineering derived parameters with time stamp, Chapter 10 PCM data packets, Chapter 7 integrated data packets, or TMoIP packets. The Ulyssix ALTAIR software suite or user custom software may also be used to seamlessly interface to the ARCHI application software for remote operation and monitoring.

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Where Technology Soars
A Woman-Owned Small Business
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ARCHI-PCM Product Features

The ARCHI-PCM is a standalone 10” x 8.5” x 3” aluminum enclosure that houses the Ulyssix 4th generation Tarsus4-PCIe card for portable and remote PCM Processing powered by USB-C power delivery (PD) using an external USB-C PD 67W AC/DC adapter, external USB battery pack or user laptop computer with USB-C power capability.

PCM Processor to Ethernet Packets

Bit Synchronizer

Designed using all DSP filter algorithms in FPGA technology for maximum performance capability

Accepts all IRIG 106 PCM code types

Bit Sync programmable input rates from 1 bps to 40 Mbps

Less than 1 dB to theoretical bit sync BER performance

All IRIG 106 codetypes are selectable for PCM output

Frame Synchronizer

Supports PCM streams from 1 bps up to 50 Mbps

Supports up to 1024 minor frames per major frame and up to 512k bits per minor frame

Frame Sync Archive capability

Advanced algorithm to allow for varying frame sizes

Decommutator

Supports all IRIG Class II decommutator features with variable word length from 3 - 64 bits, format switching, parameter concatenation and asynchronous embedded formats

High speed data transfer of user word selected channels to the PCI bus for disk storage and playback

Four on card DACs for word analog output

Full parameter math processing

PCM Simulator

Programmable PCM streams from 1 bps up to 40 Mbps

Ulyssix .tad frame sync file and Chapter 10 Archive playback capability

Fixed major frame simulator utilizing defined waveform & tabular data to output

Selectable output code type

TTL and RS-422 output capability

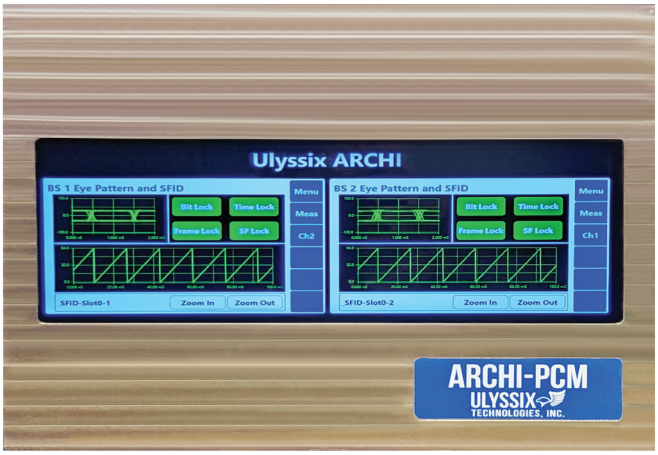
GPS or Direct IRIG Time Code Reader

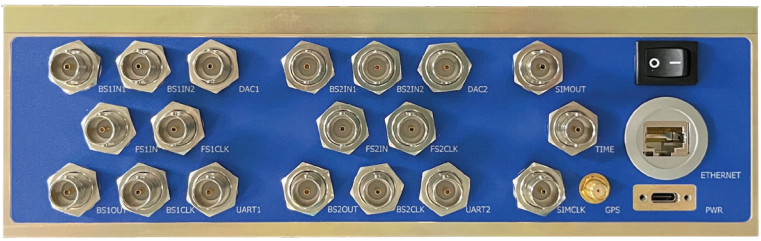
Internal GPS receiver for IRIG time reception or separate analog path onto card

Supports GPS Antenna (via SMA connector), DC level, or AM modulation input

Supports AM Modulated - IRIG A, B, G & NASA-36 and DC Input - IRIG-B DC LS/TTL

Used for both IRIG time display and/or minor frame time tag header information





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ARCHI-RF Product Features

The ARCHI-RF is a standalone 10” x 8.5” x 4” aluminum enclosure that houses the Ulyssix 4th generation Bald Eagle4-RF-PCIe card that uses the Tarsus4-PCIe card for its base. The system is powered by USB-C power delivery(PD) using an external USB-C PD 67W AC/DC adapter or external battery.

Dual RF through PCM Processing to Ethernet Packets

Main System Features

Dual Channel C/S/L/PE/P/IF bands (fully independent) FM/SOQPSK/BPSK/QPSK/GMSK

Complete RF to bits solution with Tarsus4 Mothercard connection to the Bald Eagle4 RF-PCIe daughter card in standard configuration including Dual Bit Sync/Frame Sync/Decom, PCM Simulator, IRIG Time Code Reader or GPS IRIG Time Receiver

No filter tuning or preventive maintenance required

Optional Dual Channel Modulated RF Signal Generator C/S/L/P/PE/IF bands (fully independent). Modulation Inputs are internal PCM simulator output, Chapter 10 or .tad file inputs, and external TTL Input external PCM stream

All RF N-Type connections and baseband BNC connections are directly mounted on the housing

RF Capabilities

Dual channel frequency range of C-Band (4400-5250MHz), S-Band (2185-2485 MHz), Upper-L Band (1700-1850 MHz), Lower-L Band (1420-1590 MHz), P-Band Extended (1150-1250 MHz), P-Band (200-500 MHz), 70 MHz IF

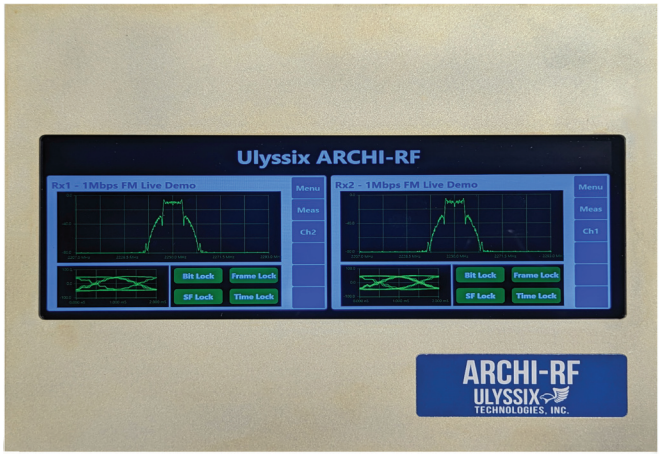
Pre-D Best Source or Optimal Ratio Diversity Combiner modes or bypass for independent dual receiver capability

Single Channel PCM modulated RF Signal Generators for simulation or BER testing at same frequencies, as stated above

RF detection performed with direct complex downconversion to DC and digitizing using single integrated IC

DSP implemented IF data bandwidth filtering from 1 kHz to 40 MHz continuous

50 kHz input frequency tuning resolution



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ARCHI-PCM Specifications

Bit Synchronizer Input Specifications

Input Data Rate	Bit Sync programmable input tunable rates from 1 bps to 40 Mbps for NRZ-L/M/S, RNRZ-L and 1 bps to 20 Mbps for Bi-Φ L/M/S
Input Source	2 independent inputs (1 single ended BNC, 1 differential Twinax)
Input Impedance	Hi-Z/75Ω/50Ω, single ended input, software selectable
Maximum Safe Input	± 35 VDC
Input Signal Level	30 mVp-p to 5 Vp-p
DC Input Level	+/- 5 VDC
Input PCM Codetypes Modes	NRZ-L/M/S, RNRZ-L, RZ, Bi-Φ L/M/S, program selectable (consult factory for other codetypes)
Derandomizer Input	RNRZ-11/15, forward/reverse, program selectable
Input Polarity	Normal, inverted or auto selectable using frame sync correlator

Bit Synchronizer Data Specifications

Loop Bandwidth	0.01% to 3.0%, to the programmed bit rate
Capture Range	+/-3 times of the programmed loop bandwidth
Data Tracking Range	+/-5 times of the programmed loop bandwidth
Sync Acquisition	less than 200 bits, typically 100 bits max
Bit Error Probability	Less than 1 dB to theoretical bit sync BER performance for bit rates up to 25 Mbps, less than 2 dB to theoretical from 25 Mbps to 33 Mbps, less than 2.7 dB to theoretical to 40 Mbps
PCM Encoder Output	TTL and RS-422 Level driven
PCM Encoder Code Types	NRZ-L/M/S, RNRZ-L, RZ, Bi-Φ L/M/S or RNRZ 11/15, program selectable
Clock Output	0°, 90°, 180°, 270°

Frame Sync/Decommutator Specifications

Input Data Rate	Up to 50 Mbps
Input Signals	TTL Level single ended, RS-422 differential or direct from Bit Sync section of the PCM Processor, NRZ-L and clock
Word Lengths	3 to 64 bits variable from channel to channel
Minor Frame Length	3 to 65,536 bits
Major Frame Length	1 to 1024 minor frames per major frame
PCM bit word order	MSB or LSB, word by word basis, program selectable
Frame Sync Pattern	16 to 64 bits
Frame Sync Location	Leading the minor frame
Frame Sync Strategy	Search-Check-Lock, programmable counts per step
Subframe Sync	FCC or SFID
Sync Error Tolerance	0 to 8 bits, program selectable
Bit Slip Window	0 to 9999 bits, program selectable
Data Polarity	Normal or inverted on a channel by channel basis
Asynchronously Embedded Formats	Supports up to 8 asynchronous embedded formats with 5 levels deep based on computer CPU capability
Bit Concatenation/Fragmented-Words	Software decommutator can combine individual bits from separate PCM words

PCM Simulator Specifications

Output Data Rate	1 bps to 40 Mbps for NRZ-x, RNRZ-L, or 20 Mbps for all others
Output PCM Codetypes	NRZ-L/M/S, RNRZ-L 11/15, RZ, Bi-Φ L/M/S, RNRZ 11/15/, forward/reverse, program selectable
Output Signal Levels	Data and Clock, TTL, and RS422 level driven
Data Words	Fixed or math functions (sine wave, triangle, square wave, sawtooth, counter) with programmable sample rate

Bit Error Rate Tester (BERT) Specification

Input Data	User selectable including PN11, PN15, simulator data or user created .bin file
Bit Rate	User selectable 1 bps to 40 Mbps
Testing Method	Each individual bit error checking with user configurable interval and cumulative readings.

DAC Output Specification

Number of Channels	2
Output Level	1 Vpp to 5 Vpp, selectable in 0.1 Vpp steps, ± 2.5V offset in 0.1 VDC steps

Time Code Reader Specifications

IRIG Codetypes	AM Modulated - IRIG A, B, G & NASA-36 DC Input - IRIG-B DC LS/TTL

ARCHI Data Storage

Storage Amount	1 TB using on board SSHD
Data Retrieval	Through supplied software suite or user generated software using Ulyssix data software driver

ARCHI Diagnostics

Version Control	All current software, firmware, and driver version numbers stored for easy retrieval
Latest Setup	Current card setup configuration is stored for verification of proper setup
Diagnostic Download	Direct download to file for transfer to Ulyssix for evaluation and recommendations

Physical Specifications

Mechanical Dimensions	10" x 8.5" x 3" Mechanical housing with internal Tarsus4-PCIe card
Interface Connectors	MDM-51 connector to individual BNC breakout cables (other configurations, consult factory)
Manufacturing	The design utilizes Surface Mount Technology (SMT), manufactured with robotic assembly techniques to IPC-610B Class 2 manufacturing standards
Temperature Range	Operating: 0°C to 70°C Storage: -20°C to 85°C
Power Consumption:	Less than 35 Watts total, for all supplies +3.3V 3.5 Amps +12V 0.8 Amps

Ordering Options

ARCHI-PCM-01	Portable Single Channel PCM Processing System powered by USB-C PD with Ethernet Interface
ARCHI-PCM-02	Portable Dual Channel PCM Processing System powered by USB-C PD with Ethernet Interface
ULX-OPT-UART	Upgrade to add 4 UART RS-232 channel outputs
ULX-OPT-CH7/CH10	Receive Chapter 7 Ethernet packets and process the Chapter 10 PCM packets within the Chapter 7 transmission. This option also allows the user to record the IRIG Chapter 10 format and playback through the archive simulator plus UDP Ethernet transmission and reception in Chapter 10 packets
ULX-OPT-CH10	Chapter 10 recording and reproducer for both Chapter 10 disk files and UDP-CH10-Ethernet packets

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Features are subject to change without notice.

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ARCHI-RF Specifications*

Receiver Specifications

Input RF Frequency Range	C-Band 4400 – 5250 MHz S-Band 2185 – 2485 MHz U/L L-Band 1420 - 1850 MHz P-Band Extended 500 - 1250 MHz P-Band 200-500 MHz IF 70 MHz
RF Inputs	2
Frequency Tuning Resolution	50 kHz
Dynamic Range	-10 dBm to -104 dBm
VSWR Ratio	2:1 typical, 2.5:1 maximum
Noise Figure	5 dB typical, 8 dB max
Maximum Safe RF Input Level	+20 dBm without damage
Input Impedance	50 ohms into SMA connectors
Spurious signal rejection	> 60 dBc

Signal Processing Specifications

IF Bandwidth	20 kHz to 56 MHz
Demodulation Modes	FM/SOQPSK/BPSK/QPSK/GMSK
Diversity Combiner	Optimal Ratio and Best Source
Combiner Mode	Pre-D
AFC Tracking	Maximum AFC acquisition range is +/- 50 MHz for C and S Band; +/- 25 MHz for L-Band; +/- 12.5 MHz for EP Band; +/- 6.25 MHz for P-Band/IF 70 MHz
AFC Frequency Resolution	1 kHz for all bands
AFC Acquisition	≤ 100 msec for all bands
AGC Time Constants	1.0 msec, 0.1msec, 0.01msec, selectable
AGC Modes	Automatic, Manual, Freeze
AM AGC Out	AC coupled AM AGC detector output, 50 kHz frequency response, 5 Vpp bipolar or unipolar out
AGC DC Level Detector	DC coupled from 0 to + 3.5 VDC for min to max RF AGC attenuation

Physical Specifications

PCIe Form Factor	100 mm x 160 mm (3U)
Interface Connectors	RF inputs, RF Signal Generator Outputs: SMA, Video Outputs and AGC Testpoints are BNC outputs from the Tarsus4 MDM-51 DAC outputs connectors
Manufacturing	The design utilizes Surface Mount Technology (SMT), manufactured with robotic assembly techniques to IPC-610B Class 2 manufacturing standards
Temperature Range	Operating: 0°C to 50°C Storage: -20°C to 60°C
Power Consumption:	Approximately 30 Watts total, for all supplies
Chassis Slots per Card	Three (3) slots
Mechanical Dimensions	100 mm height, 160 mm length, 28 mm width (not including mounting or edge connectors) (3U)

Ordering Options

Bald Eagle4 RF-PCIe	C-Band, S-Band, Upper L-Band, Lower L-Band, P-Band extended, P-Band supporting data rates to 40 Mbps full RF to bits including dual receivers, dual bit sync with Multi-Symbol Detector/frame sync/decom, PCM simulator, IRIG Time Code Reader in half length PCIe form factor
ULX-OPT-UART	Upgrade to add 4 UART RS-232 channel outputs
ULX-OPT-CH7/CH10	Receive Chapter 7 Ethernet packets and process the Chapter 10 PCM packets within the Chapter 7 transmission. This option also allows the user to record the IRIG Chapter 10 format and playback through the archive simulator plus UDP Ethernet transmission and reception in Chapter 10 packets
ULX-OPT-CH10	Chapter 10 recording and reproducer for both Chapter 10 disk files and UDP-CH10-Ethernet packets

RF Generator Specifications (Optional)

ULX-OPT-Bald Eagle4-TX	Optional Single RF Signal generators with RF C/S/L/P/EP/IF Frequency Bands and BERT Eb/N0 error analysis capability
Output RF Frequency Range	C-Band 4400 – 5250 MHz S-Band 2185 – 2485 MHz Upper L-Band 1700 – 1850 MHz Lower L-Band 1420 – 1590 MHz P-Band Extended 500 –1250 MHz P-Band 200– 500 MHz IF 70 MHz
Transmit Outputs:	1
IF Bandwidth	1 kHz to 40 MHz
Modulation Modes	FM/SOQPSK/BPSK/QPSK/GMSK
Modulation Source	Tarsus4 PCM simulator running stored PN-11/15 patterns, user defined PCM frame, archived user data, or external TTL Input PCM stream
Output Dynamic Range	-20 dB to -90 dB
Output Impedance	50 ohms using SMA connector

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