Tarsus4-PCIe

40 Mbps PCM Processor - Single or Dual Version

Form / Fit / Function Upgrade to the Ulyssix Tarsus3-PCIe

Bit Sync / Frame Sync / PCM Decommutator / GPS or Direct IRIG Time Code Reader / PCM Simulator / Bit Error Rate Tester (BERT)

ULYSSIX TECHNOLOGIES, INC.

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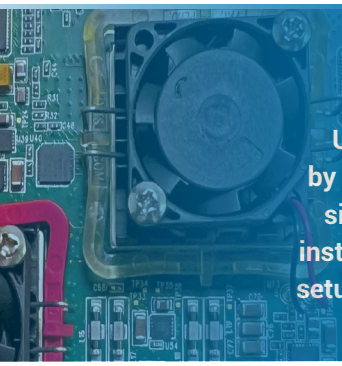


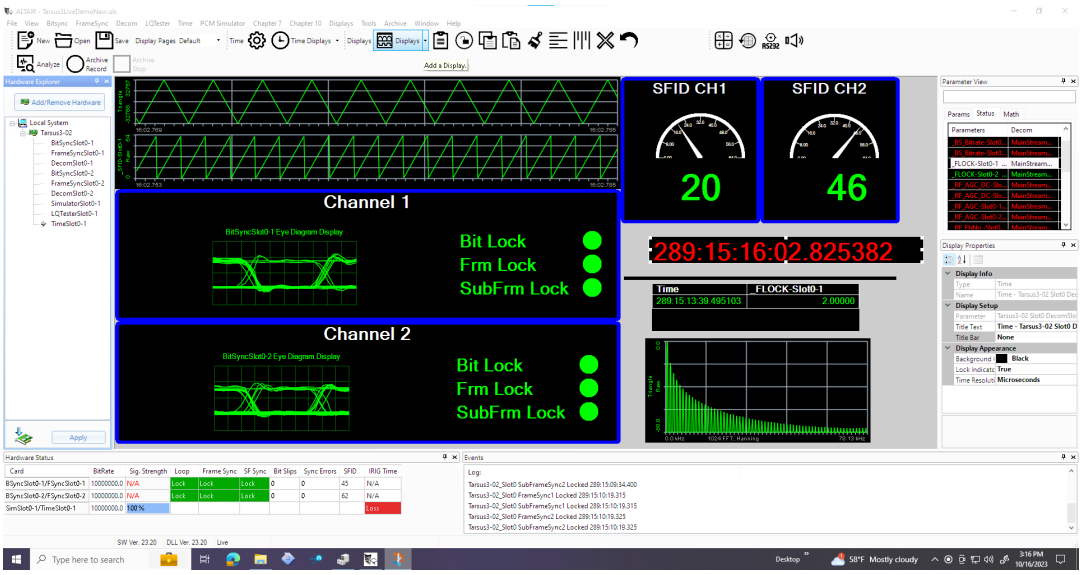
Tarsus4-PCIe

Ulyssix's 4th generation PCM processor, the Tarsus4, advances Ulyssix's PCM processing capability by utilizing the PCIe form factor to integrate a single or dual PCM bit sync/frame sync/decommutator/ simulator/GPS Receiver/IRIG time code reader in the same housing with other test and measurement instrumentation (i.e., frame grabber, signal conditioning, spectrum analyzers, etc.). The Tarsus4 can be setup and controlled using the Ulyssix ALTAIR software or custom software easily written using Ulyssix supplied drivers and .dll.

ULYSSIX ALTAIR Software Suite

Including:
Tarsus4 setup
Real-Time Data Acquisition with Graphical Monitoring
Extensive Math Capability
Fully designed and supported at Ulyssix in USA

Optional:
IRIG CH10 Recorder/Playback
UDP Frame and Parameter Broadcasting
UART PCM Output
LQ Tester/BERT Function
IRIG Ch7 Ethernet Packet Receiver



Bit Synchronizer

Designed using all DSP filter algorithms in FPGA technology for maximum performance capability

Accepts all IRIG 106 PCM code types

Bit Sync programmable input rates from 1 bps to 40 Mbps

Less than 1 dB to theoretical bit sync BER performance

All IRIG 106 codetypes are selectable for PCM output

Frame Synchronizer

Supports PCM streams from 1 bps up to 50 Mbps

Supports up to 1024 minor frames per major frame and 16 Mb per minor frame

Frame Sync Archive capability

Advanced algorithm to allow for varying frame sizes

Decommutator

Supports all IRIG Class II decommutator features with variable word length from 3 - 64 bits, format switching, parameter concatenation and asynchronous embedded formats

High speed data transfer of user word selected channels to the PCI bus for disk storage and playback

Two on card DACs for word analog output

Full parameter math processing

Available with two different user friendly Windows GUI based software suites for full setup of format frame, word selection, channel display capability, and optional client/ server capability

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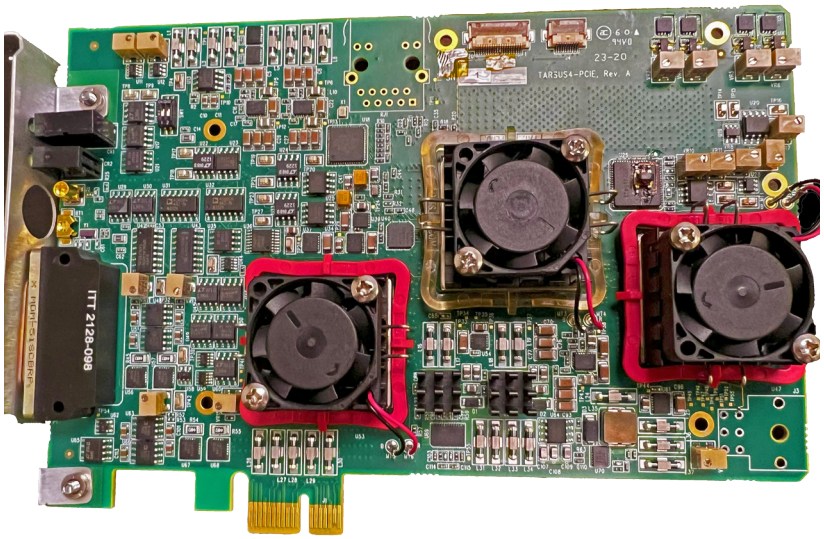
Tarsus4-PCIe

The Tarsus4 PCM Processor board is powered by the latest Intel Cyclone 10 GX FPGAs with the firmware being user reconfigurable using Ulyssix supplied FlashBurn software with user upgrade capability under maintenance contract. The Tarsus4 is the mothercard to mount the optional Bald Eagle RF daughter card which includes dual receiver with diversity combiner capability, with optional transmitter/frequency converter capability allowing the user to have a complete RF to bits with real-time and post analysis PCM decommutator system in a single board set.



GPS or Direct IRIG Time Code Reader

Internal GPS receiver for IRIG time reception or separate analog path onto card

Supports GPS Antenna (via SMA connector), DC level, or AM modulation input

Supports AM Modulated - IRIG A, B, G & NASA-36 and DC Input - IRIG-B DC LS/TTL

Used for both IRIG time display and/or minor frame time tag header information

PCM Simulator

Programmable PCM streams from 1 bps up to 40 Mbps

Ulyssix .tad frame sync file and Chapter 10 Archive playback capability

Fixed major frame simulator utilizing defined waveform & tabular data to output

Forward Error Corrected output capable

Selectable output code type

TTL and RS-422 output capability

Diagnostics

Diagnostic feature used to aid Ulyssix in troubleshooting FPGA firmware internal control register configuration from user setup configuration

Retrieval popup form in ALTAIR software suite outputs diagnostic file for transfer to Ulyssix for quick system analysis for card configuration errors, setup errors, or actual hardware failures

Tarsus4 Specifications

Bit Synchronizer Input Specifications

Input Data Rate	Bit Sync programmable input tunable rates from 1 bps to 40 Mbps for NRZ-L/M/S, RNRZ-L and 1 bps to 20 Mbps for Bi-Φ L/M/S
Input Source	2 independent inputs (1 single ended BNC, 1 differential Twinax)
Input Impedance	Hi-Z/75Ω/50Ω, single ended input, software selectable
Maximum Safe Input	± 35 VDC
Input Signal Level	30 mVp-p to 5 Vp-p
DC Input Level	+/- 5 VDC
Input PCM Codetypes Modes	NRZ-L/M/S, RNRZ-L, RZ, Bi-Φ L/M/S, program selectable (consult factory for other codetypes)
Derandomizer Input	RNRZ-11/15, forward/reverse, program selectable
Input Polarity	Normal, inverted or auto selectable using frame sync correlator

Bit Synchronizer Data Specifications

Loop Bandwidth	0.01% to 3.0%, to the programmed bit rate
Capture Range	+/-3 times of the programmed loop bandwidth
Data Tracking Range	+/-5 times of the programmed loop bandwidth
Sync Acquisition	less than 200 bits, typically 100 bits max
Bit Error Probability	Less than 1 dB to theoretical bit sync BER performance for bit rates up to 25 Mbps, less than 2 dB to theoretical from 25 Mbps to 33 Mbps, less than 2.7 dB to theoretical to 40 Mbps
PCM Encoder Output	TTL and RS-422 Level driven
PCM Encoder Code Types	NRZ-L/M/S, RNRZ-L, RZ, Bi-Φ L/M/S or RNRZ 11/15, program selectable
Clock Output	0°, 90°, 180°, 270°

Frame Sync/Decommutator Specifications

Input Data Rate	Up to 50 Mbps
Input Signals	TTL Level single ended, RS-422 differential or direct from Bit Sync section of the PCM Processor, NRZ-L and clock
Word Lengths	3 to 64 bits variable from channel to channel
Minor Frame Length	3 to 16,777,216 bits
Major Frame Length	1 to 1024 minor frames per major frame
PCM bit word order	MSB or LSB, word by word basis, program selectable
Frame Sync Pattern	16 to 64 bits
Frame Sync Location	Leading the minor frame
Frame Sync Strategy	Search-Check-Lock, programmable counts per step
Subframe Sync	FCC or SFID
Sync Error Tolerance	0 to 8 bits, program selectable
Bit Slip Window	0 to 9999 bits, program selectable
Data Polarity	Normal or inverted on a channel by channel basis
Asynchronously Embedded Formats	Supports up to 8 asynchronous embedded formats with 5 levels deep based on computer CPU capability
Bit Concatenation/Fragmented-Words	Software decommutator can combine individual bits from separate PCM words

PCM Simulator Specifications

Output Data Rate	1 bps to 40 Mbps for NRZ-x, RNRZ-L, or 20 Mbps for all others
Output PCM Codetypes	NRZ-L/M/S, RNRZ-L 11/15, RZ, Bi-Φ L/M/S, RNRZ 11/15/, forward/reverse, program selectable
Output Signal Levels	Data and Clock, TTL, and RS422 level driven
Data Words	Fixed or math functions (sine wave, triangle, square wave, sawtooth, counter) with programmable sample rate

DAC Output Specification

Number of Channels	4
Output Level	1 Vpp to 5 Vpp, selectable in 0.1 Vpp steps, ± 2.5V offset in 0.1 VDC steps

Time Code Reader Specifications

IRIG Codetypes	AM Modulated - IRIG A, B, G & NASA-36 DC Input - IRIG-B DC LS/TTL

On Card Data Storage - 1 Optional

Storage Amount	Up to 32 GB archived data stored in 32-bit packed format
Data Retrieval	Through supplied software suite or user generated software using Ulyssix data software driver

Tarsus4 Diagnostics

Version Control	All current software, firmware, and driver version numbers stored for easy retrieval
Latest Setup	Current card setup configuration is stored for verification of proper setup
Diagnostic Download	Direct download to file for transfer to Ulyssix for evaluation and recommendations

Physical Specifications

Mechanical Dimensions	PCIe 3U form factor, 100 mm height, 160 mm length, 28 mm width (not including mounting or edge connectors), PCIe short card configuration
Interface Connectors	MDM-51 connector to individual BNC breakout cables (other configurations, consult factory)
Manufacturing	The design utilizes Surface Mount Technology (SMT), manufactured with robotic assembly techniques to IPC-610B Class 2 manufacturing standards
Temperature Range	Operating: 0°C to 70°C Storage: -20°C to 85°C
Chassis Slots per Card	Two (2) Slots
Power Consumption:	Less than 25 Watts total, for all supplies +3.3V 3.5 Amps +12V 0.8 Amps

Ordering Options

Tarsus4-PCIe-01	PCM Processor Card 40 Mbps Bit Sync, Frame Sync, Decom, IRIG Time Code Reader and PCM Simulator with Tarsus PCM Software Application
Tarsus4-PCIe-02Dual	40 Mbps Dual Bit Sync, Dual Frame Sync, Dual Decommutator, IRIG Time Code Reader, and PCM Simulator with ALTAIR PCM Software Application
Bald Eagle RF4	Dual Receiver with Diversity Combiner C/S/Upper-L/Lower-L/P-Band daughter card mounted to the Tarsus4 card. (see Bald Eagle RF for details)
Bald Eagle RF4-TX	Dual Receiver with Diversity Combiner C/S/Upper-L/Lower-L/P-Band with All Band RF transmitter/RF modulator/frequency converter daughter card mounted to the Tarsus4card. (see Bald Eagle RF brochure for details)
ULX-OPT-UART	Upgrade to add 4 UART RS-232 channel outputs
ULX-OPT-CH7/CH10	Receive Chapter 7 Ethernet packets and process the Chapter 10 PCM packets within the Chapter 7 transmission. This option also allows the user to record the IRIG Chapter 10 format and playback through the archive simulator plus UDP Ethernet transmission and reception in Chapter 10 packets
ULX-OPT-CH10	Chapter 10 recording and reproducer for both Chapter 10 disk files and UDP-CH10-Ethernet packets
ULX-OPT-LQTESTER	BERT Tester Option for Time Latency Measurements and Bit Error Tester of PCM Data Stream
ULX-OPT-UDP PARAM/FRAME BROADCAST	UDP Frame and/or decom parameter mulitcast or unicast broadcast for external Altair software networking or external data transfer

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Specifications are subject to change without notice.
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