# DSP IP's Give the Ability to Use Programmable Filtering and Frequency Synthesization in Telemetry Applications

Glenn K. Rosenthal
President
Ulyssix Technologies, Inc.

Telemetry applications have the need for a wide frequency range of baseband subcarrier demodulators (300 Hz - 4 MHz) with different types of modulation techniques (FM, PM, BPSK, QPSK) for high data rates (above 20 kHz). Frequency translators and data filters comprise the two main building blocks of all types of data demodulators. The traditional design approach for high-speed data applications uses fixed frequency voltage controlled oscillators (VCOs) and analog filters designed with active and passive components. This traditional approach results in designs are not programmable but are selectable from predetermined fixed frequencies and designs that vary from both temperature and time causing major setup and calibration issues for the end user.

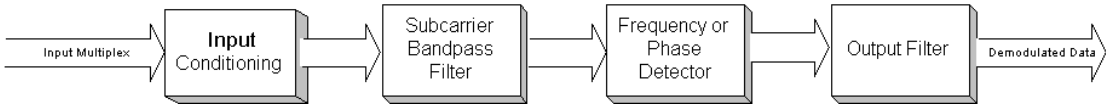


Fig. 1 - Traditional Telemetry Demodulator

Traditional telemetry demodulators (see fig 1) are customer frequency specified and supplied to the market with both frequency bandpass and output filters. In order to change the demodulator frequency, a filter module must be either relay switched in or replaced. Of course, this process is very time consuming and inaccurate because of the nature of analog components.

Because of all the different types and frequency range of subcarriers that need to be acquired, the development of a fully digital signal processing (DSP) based demodulator is essential for the telemetry user. By developing intellectual properties (IP's) for the implementation of the demodulator digital algorithms for use in standard off-the-shelf field programmable gate arrays (FPGA), a new generation of extremely flexible multi type demodulators can be developed for the telemetry market. Using this approach, the Syrinx family of demodulators was developed using Altera FPGA architecture.

In order to successfully achieve the design goals of the Syrinx family, three unique DSP IP's were developed. These IP's included an 8-stage recursive FIR decimation filter, a 32-tap FIR filter and a modulated numerical controlled oscillator (MNCO) with quadrature output. The ability to capture an extremely wide range of varies types of modulated subcarrier comprises the key component for any telemetry demodulator. DSP FIR filters IP's with extremely precise cutoff frequencies and excellent distortion characteristics achieve this goal..

The problem of creating a wide cutoff varying flat filter in the passband with good attenuation in the reject band constantly plagues most DSP filter designers. In the Syrinx demodulators, the filter cutoff frequency must vary from 0.0008 to 0.2 of the sample rate ($F_s$) of 10 MHz. As most DSP designers know, to achieve a FIR filter with this very low cutoff frequency, the filter must use several thousand taps. Running that many taps at 10 MHz sample isn't achievable, so a different technique must be used. The design technique used in the Syrinx created an IP for an 8-stage decimation filter with another IP for a 32-tap FIR filter running with 4 parallel multipliers. Using this technique, these two IP's running together can achieve together any filter frequency capability from 0.0008 $F_s$ to 0.2 $F_s$.

The first DSP filter IP is the 8-stage decimation filter which contains a 16 tap FIR half-band filter with internal storage capability to decimate (throw away every other data point) and parallel shift register to store the decimated data. A multiplexing state machine to recursively feed the data back into the half-band

filter achieves the final function in the IP. Since only half the data is ever used for the output of the decimation filter, only every other group of synchronize data must be fed into the half-band filter. Therefore, a "hole" in time always occurs which allows another stage of data to be filter and decimated as long as the data being fed through the half-band filter constantly runs at the input sample rate.

Figure 2 shows the data flow through the decimation filter for 4 stages of decimation. The one aspect that must be remembered is that the data fed into the half-band filter must follow the Sampling Theorem, which states that time synchronize data must be maintained. The decimation filter IP is used to slow down the sampled rate of the data so that the sample rate going into the 32-tap FIR filter will always be between 0.1 and 0.2 of the desired filter frequency. This must be done without creating distortion in the passband while eliminating any higher frequency terms that will alias the data during the decimation process.

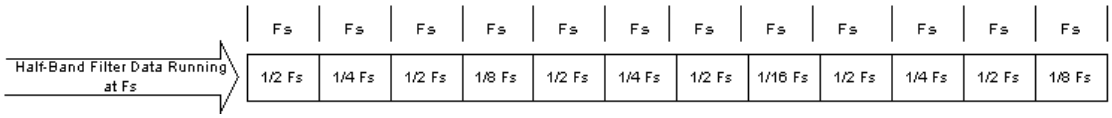


Fig. 2 - Decimation Filter IP Data Flow

The second stage of the varying demodulator filter is another DSP IP containing a 32-tap FIR filter with 4 parallel multiply accumulators (MACs). By using 4 parallel multipliers, this IP can achieve the data throughput capability by running the MACs at only 4 times the sample rate where by using only a single multiplier; the MAC rate would have to be at 16 times the sample rate. Figure 3 shows the frequency response of the IP using 12-bit coefficient resolution. Notice that the passband ripple is held to less than 0.1 dB of ripple with the reject band being 2 times cutoff at -60 dB. The filter coefficients are loaded into static RAM in the FPGA through bi-directional data lines for ease in reconfiguring the filter frequency response.

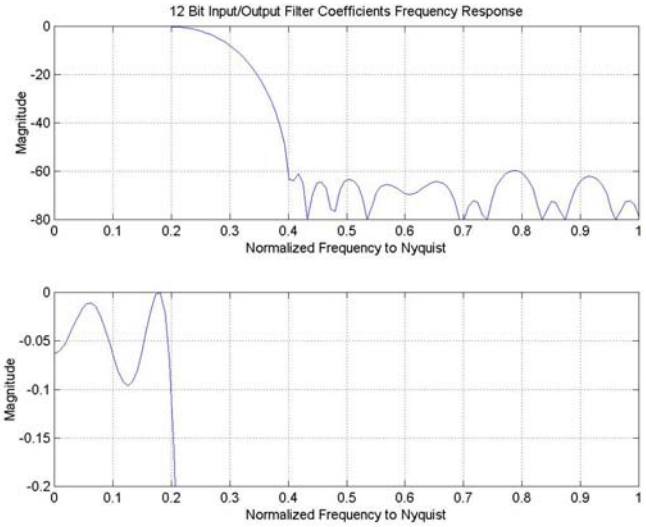


Fig. 3 - 32 TAP FIR Filter Frequency Response

By combining both the decimation filter IP and the 32-tap FIR filter IP in the Syrinx, the frequency response for the demodulator filters is essentially identical from .0008 $F_s$ to 0.2 $F_s$. Since the filter algorithms are created in IP's to be placed into FPGA components, another decimation IP could be added to achieve varying filter rates now from 0.000003 $F_s$ to 0.2 $F_s$.

The MNCO comprises the other major DSP IP building block created for the Syrinx digital demodulator (fig. 4). The MNCO IP is designed to create SIN and COS outputs, in exact quadrature over a range of 250 Hz to 4 MHz with resolution to 0.0039 Hz. Using a 32-bit phase accumulator achieves the wide range of frequency synthesization and the high degree of frequency resolution. Prior to the phase accumulator, a parallel digital multiplier modulates the downconverter by an input waveform. This feature allows the

downconverter to be used in a phase lock loop application to complete the Costa's Loop for phase demodulation.

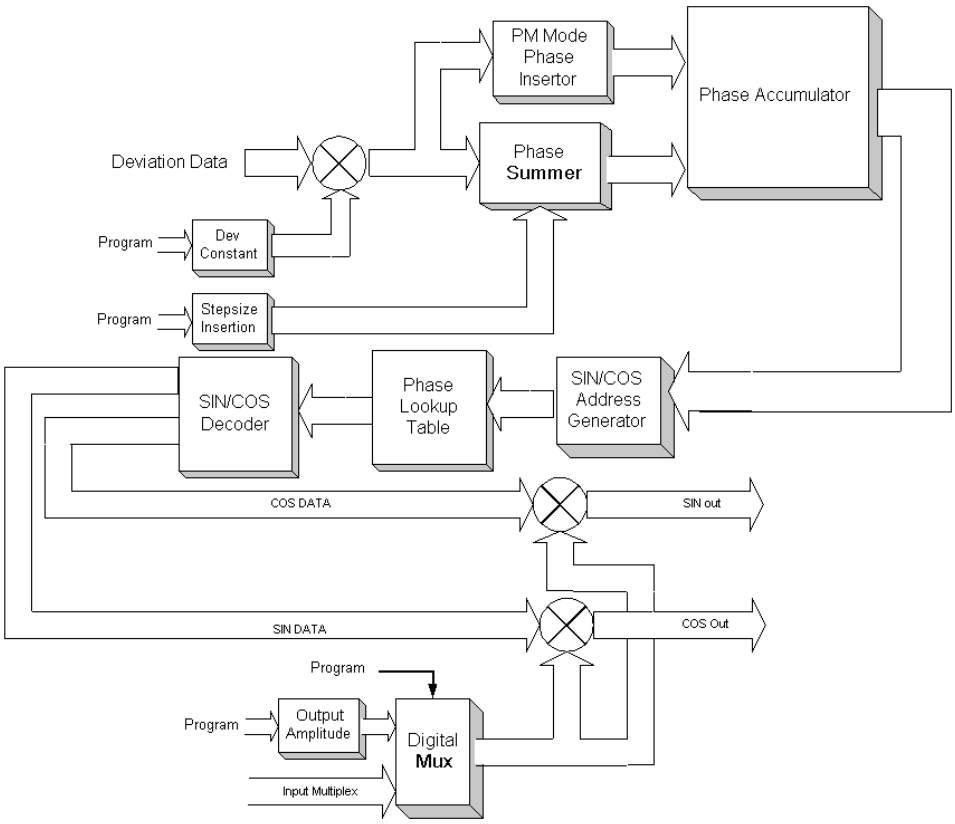


Fig. 4 - Complex Modulated Numerical Controlled Oscillator

The MNCO creates the quadrature output using a 90° SIN lookup table stored in the IP. The stored first quadrant sinewave feeds into address and data decoding conversion circuitry to invert the address and sign bits creating the entire 360° sinewave. In parallel, the IP contains circuitry to 90° phase shift the sinewave to create the quadrature cosine waveform. Since both waveforms are created from the same phase accumulator driven from the same oscillator, the waveforms must remain in perfect quadrature. On the output of each waveform generator are parallel multipliers that are used as the downconverter mixers. In this manner, the entire complex downconversion algorithm for the frequency demodulation algorithm is contained in this IP. The outputs of the MNCO are two 12 bit sine and cosine data busses. By creating the quadrature outputs in the IP, the Syrinx demodulator can use low pass filters in the place of the traditional bandpass filters.