

# A DSP IMPLEMENTED DIGITAL FM MULTIPLEXING SYSTEM

Glenn K. Rosenthal

Metraplex Corporation  
5305 Spectrum Drive  
Frederick, Md. 21701  
301-662-8000

## ABSTRACT

Recent advancements in high-speed Digital Signal Processing (DSP) concepts and devices permit digital hardware implementation of relatively high-frequency signal processing, which formerly required analog circuitry. Systems utilizing this technology can provide a high degree of software programmability; improved reproducibility, reliability, and maintainability; immunity to temperature induced drift errors; and compare favorably in cost to their analog counterparts.

This paper describes the DSP implementation of a software programmable, digital frequency multiplexed FM system providing up to 4 output multiplexes, containing up to 36 subcarrier channels extending up to 4 MHz, and accommodating modulating frequencies up to 64 kHz. System overall design goals and the implementation of these goals are presented.

Key Words : Frequency Modulation, Numerical Controlled Oscillator, Digital Pipeline Design.

## OVERALL SYSTEM DESIGN GOALS

The Digital Frequency Multiplexer (DFM) overall system design goal is to replace existing wide band analog frequency modulation (FM) data recording equipment with a digitally implemented, fully programmable alternative. Instead of using the classical approach of generating an FM subcarrier by charging and discharging a timing capacitor circuit and then shaping the output triangle to remove the odd order harmonics, the DFM approach generates the subcarriers using a computer programmable digital frequency synthesizer clocked by an extremely stable crystal source. Since the DFM subcarriers are digitally generated using the stable clock

source, it is not necessary to calibrate the frequency of the subcarriers over time and temperature changes.

A straight forward approach was taken in selecting the design features of the DFM. Start with the standard features provided in analog FM systems used for wide band recording (e.g., differential inputs, gain and offset control), then add the features of a digital synthesizer and computer control (programmable center frequencies, deviations, pre-emphasis, multiplex configurations, etc.).

The resulting DFM design has inputs and outputs that are in analog format. Data frequencies at the input can be up to 64 kHz, and the output multiplexes can have bandwidths up to 4 MHz with capability to drive both multi-track analog tape recorders and fiber optic links.

The heart of each channel of the DFM is a proprietary application specific integrated circuit (ASIC) gate array that performs the digital synthesis and modulation of the each subcarrier. Each modulated subcarrier employs an ASIC that is synchronized from one system clock. In this manner, all subcarriers are perfectly timed to one another prior to and during multiplexing. The digitizing of each data channel is also synchronized off the same clock, ensuring exact time correlation between all the channels in a multiplex.

The physical configuration of the DFM is also based on expanding the present capabilities of an analog FM data recording systems. A complete DFM subsystem fits in an 8.75" by 19" rack mount housing. Each DFM subsystem (Figure 1) contains up to 36 independent data channel digital modulators, with 4 modulators located on each card. The output of each digital modulator can be assigned to one of four digital multiplexers and then converted to analog format for storage or transmission. A reference frequency and common data channel (e.g., voice) can also be multiplexed into any or all of the multiplexes. The DFM system is expandable and can contain up to 14 subsystems, all controlled from one of three sources: locally via the unit's electroluminescent (EL) graphic display with infra-red touch screen user interface, or remotely either by an IBM-PC compatible computer or by a host computer with GPIB or RS-232 interface.

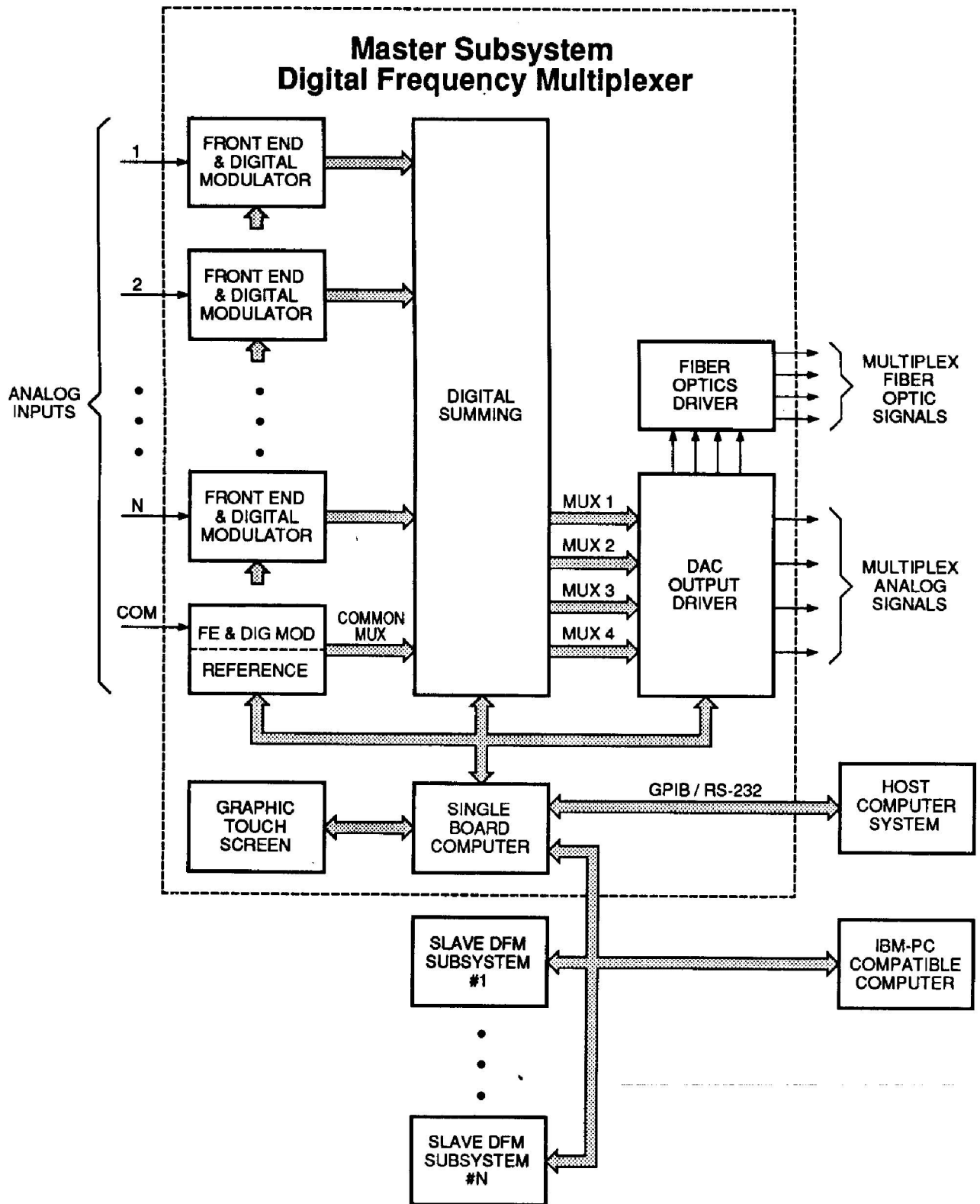


Figure 1. Digital Frequency Multiplexer System Architecture

## DESIGN IMPLEMENTATION DESCRIPTION

Each multiplex in a DFM system can be broken down into five sections: input data front end, digital modulator, digital summing or multiplexing, analog reconstruction, and the controlling computer. Each section is designed with all features being computer programmable, in contrast to analog FM systems that use manual adjustments (i.e., potentiometers and switches). The following topics describe each section of the DFM and compare the techniques used in the DFM with those in analog FM recording systems.

### Input Data Front End

The input data front end accepts either analog single ended or differential inputs (Figure 2). The input is received by a differential buffer circuit that can accommodate data bandwidths up to 64 kHz, common mode voltages up to 200 V DC, and voltage inputs up to 10 V pp. The output of the buffer is connected to an analog switch. The switch is used to isolate the input data signal from the rest of the circuit when performing an internal offset correction to automatically balance the channel.

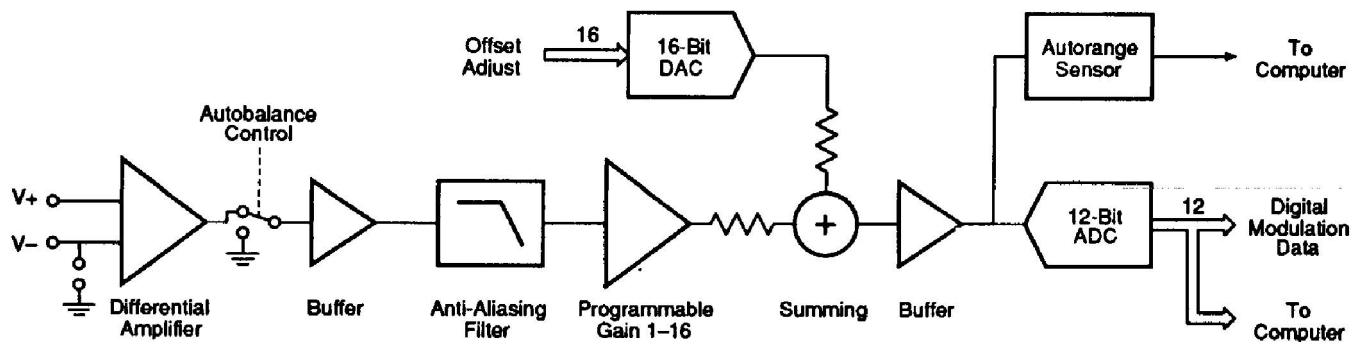


Figure 2. DFM Channel Front End

The input data signal is then buffered and filtered by a lowpass anti-aliasing filter, which accomplishes two things. First, it filters the data above 64 kHz before sampling. This is necessary because if the data is not band limited prior to sampling, the digital data spectrum will be corrupted by any frequency terms above the Nyquist rate of the sampling system.

Second, the filter corrects for the  $\sin(x)/x$  attenuation effects caused by the sampling process. Most digitizing systems do not attempt to make such corrections. Since the data signal is sampled with pulses of finite width and not with ideal zero-width impulse functions, the resulting signal will be attenuated by a  $\sin(x)/x$  or  $\text{sinc}(x)$  factor, causing the amplitude of the sampled data to decrease as the data frequency

increases.<sup>(1)</sup> Therefore, by adding a  $\sin(x)/x$  correction to the anti-aliasing filter, the same fixed frequency anti-aliasing filter and fixed frequency sampling system can be used for all input data frequencies.

After the anti-aliasing filter, the data is passed to a programmable gain amplifier (PGA). This amplifier is computer controlled by user input selection to allow input data voltages from 0.5 V<sub>pp</sub> to 8.0 V<sub>pp</sub>, in binary gain increments, for  $\pm 100\%$  subcarrier deviations. This corresponds to the gain adjustment potentiometer found in standard analog FM systems.

The output of the PGA is current summed together with a user programmable offset correction that allows the input data to be either unipolar or bipolar, with or without any DC offset. A 16-bit digital to analog converter (DAC) supplies the offset correction, and is also used by the computer to remove any offsets in the analog front end. During an automatic balance sequence, the computer grounds the input to the data channel, by switching the previously discussed analog switch after the input buffer, and reads the sampled data. The offset is measured after sampling and is added to the user selected offset at the DAC. This internal zeroing eliminates the need to calibrate each subcarrier prior to performing a test. On current analog FM systems, the offset adjustment is performed either by turning a potentiometer or running an automatic calibration sequence. This DAC controlled offset adjustment is also used to perform pre- and post-calibration sequencing of each data channel. Because the computer controls the offset values sent to the offset DAC, the number of steps and the dwell time of each step are user selectable.

Finally, the input data is digitized using a 12-bit sampling analog to digital converter (ADC). The ADC has a full input range of  $\pm 5$  V DC. By defining that an input voltage range of 8 V<sub>pp</sub> corresponds to a  $\pm 100\%$  subcarrier deviation, each data channel can actually be deviated  $\pm 125\%$ , providing a safety margin for overdeviated input signals. The ADC is clocked at approximately 330 kHz, which gives a minimum of 5 points per period for the fastest input frequency of 64 kHz. The ADC clock is derived from the system clock so that all data within the digital pipeline is fully synchronized.

The input to the ADC is also sampled by an automatic ranging circuit. This circuit senses the RMS level of the input data to the ADC and allows the computer to change the gain of the PGA if the full input range of the ADC is not being used.

The digital output of the ADC is the modulation source for the digital modulator. The computer has the ability to read the modulation data and display a representation of the data on the EL panel. This feature provides the user with an indication whether the input data front end is set up correctly to produce the correct amount of subcarrier

deviation. Adjustments can be performed by the user to the programmable front end features while the modulation data is being displayed, which gives the user immediate feedback to the changes taken.

## Digital Modulator

All the hardware algorithms necessary to perform the digital frequency modulation of a subcarrier are built into the ASIC. Figure 3 illustrates the FM portion of the ASIC. The subcarrier frequency is generated using a numerically controlled oscillator (NCO). The ASIC is programmed with the user selected subcarrier parameters: center frequency, deviation range, and pre-emphasis. After these values are sent to the ASIC, the ASIC performs all subcarrier generation and modulation without computer intervention. The only time the computer communicates to the ASIC is when the user changes a subcarrier parameter.

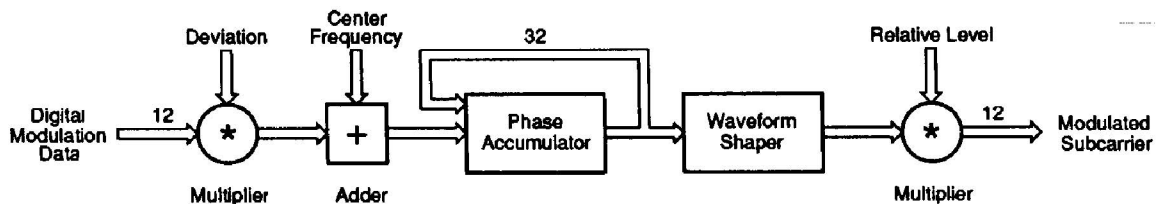


Figure 3. Frequency Modulation Section of the ASIC

The output of the ADC is registered and fed into the modulation data input of the ASIC. All data inside and outside the modulator is pipeline registered. This means after a function is performed (summing, multiplying, decoding, etc.) the data is clocked into a register that maintains synchronization of the digital pipeline. All data channels have the same number of pipeline delays, so all data from channel to channel will be perfectly time correlated.

The digital input modulation data is scaled by a digital multiplier with a computer calculated value from the user selected deviation range of the subcarrier. The ASIC is designed to allow deviation scaling from 0.5% to 50.0% of the selected center frequency of a subcarrier. Therefore, as different deviation values are chosen, the deviation multiplier scales the ADC data to allow 12-bit resolution (4096 unique steps).

After the modulation data is scaled for deviation, the data is summed with a user selected center frequency value. The user can select any subcarrier frequency from 300 Hz to 4 MHz. The computer calculates the appropriate value to obtain the desired subcarrier center frequency.

The output of the center frequency summer is fed into a phase accumulator, which is the heart of the NCO. The input data to the accumulator represents the phase step for each clock cycle, and the output of the phase accumulator at any time corresponds to the phase of the programmed frequency. The accumulator overflows between 359 and 0 degrees, and the rate at which the accumulator overflows is equal to the output rate of the subcarrier. The phase accumulator inside the ASIC is 32 bits wide and is synchronized to the system clock which is running at  $2^{24}$  Hz. The frequency resolution of the phase accumulator is equal to the clock frequency divided by the number of bits in the accumulator, yielding  $2^{-8}$  or 3.9 millihertz.<sup>(2)</sup>

The output of the phase accumulator, which represents the phase of the waveform being synthesized, is converted to a sine wave in the wave shaping section. This section calculates the true value for the sine wave at the phase angle that is being entered. By calculating the true value of the sine wave and having a crystal controlled phase accumulator with excellent phase resolution, there are essentially no harmonic distortion terms generated in the sine wave, as there are in present analog wideband FM recording systems. The output from the waveform shaper is a 12-bit full scale digital sine wave value that is then scaled against a user entered relative output level, or pre-emphasis value. Pre-emphasis scaling is done using a 12 x 12-bit, twos complement multiplier. Entering 0 dB for the pre-emphasis value leaves the digital sine wave at full scale. The user can program the pre-emphasis value of each subcarrier from 0 dB to -20 dB.

## DIGITAL SUMMING

The digital summing section multiplexes together the user selected subcarriers. As previously stated, each DFM subsystem can have up to 36 data channels plus 2 channels in a common multiplex. These channels can be configured for output in up to 4 different multiplexes. Table 1 illustrates the different configurations, listing the number of channels for each output multiplex.

Four data channel front ends and digital modulators are placed on one printed circuit board. Their outputs are digitally summed together prior to exiting the board by a second proprietary ASTC. This approach greatly reduces the number of connection lines within the DFM subsystem, so that only 12 data lines for each of the four channels are required.

After the initial summed data is received, the hardware is designed to direct the different digital subcarriers to the appropriate summing points for the desired multiplex configuration. The second ASIC was also designed to have the flexibility to program different pipeline delays in the summing system in order to maintain time

Table 1. DFM Multiplex Configuration

Configuration	Maximum Number of Channels per Multiplex			
	Mux 1	Mux 2	Mux 3	Mux 4
1	8	8	8	8
2	12	12	12	
3	16		20	
4	8	8	20	
5	12	24		
6	32			

correlation between all subcarriers in all the different multiplex configurations. Each multiplex has a selection control register that is computer programmed to turn on or off the common multiplex and to direct the multiplexed subcarriers to the appropriate multiplex outputs.

### ANALOG RECONSTRUCTION

Analog reconstruction of the digitally multiplexed subcarriers is accomplished using a high speed 12-bit DAC (Figure 4). The DAC has a settling time twice as fast as the rate that data is processed in the pipeline. The DAC must also be able to output a bipolar sine wave without causing distortion terms induced into the multiplexed subcarriers. During the DAC conversion, the system clock frequency is modulated with the frequency of the digitally synthesized subcarrier. The digital system clock frequency term is removed from the multiplex using a lowpass interpolation filter. This filter has a passband from DC to 4 MHz and provides excellent attenuation at the digital pipeline rate of  $2^{24}$  or approximately 16 MHz. The interpolation filter also provides a constant group delay through the passband of the filter in order not to cause time correlation errors within the multiplexed subcarrier data.

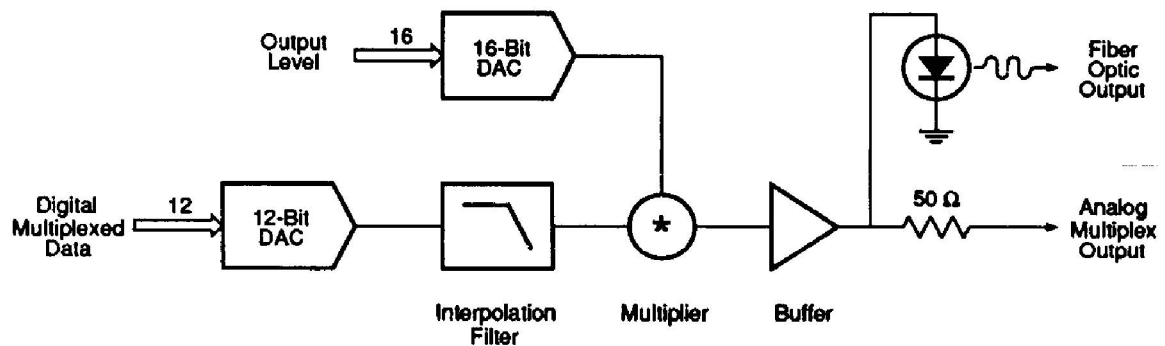


Figure 4. Analog Reconstruction



Each filtered, reconstructed multiplex output is passed to a bipolar analog multiplier. The user can program the output level of each multiplex to the appropriate level for the tape recorder system that the data will be stored on. A 16-bit DAC programmed by the computer is used to generate the scale factor to multiply the multiplexed subcarriers. This programmable multiplex output level is similar to adjusting a potentiometer on the output section of a present analog FM recording data systems.

Each output scaled multiplex is available from the DFM subsystem in two different forms: as a 50-ohm driven output on a BNC connector, or as a fiber optic output on an SMA connector. The fiber optic output is ideal for performing real time demodulation of the data within a kilometer of the DFM subsystem.

## SUMMARY

Now there is an alternative to analog wideband FM data recording systems. The day of plug-in replacements for multiplex system reconfiguration is gone. Subcarriers, multiplex configurations, and input/output levels are now completely programmable. No longer is there a need to recalibrate for temperature and time variations. All data channels now have the same stability as the crystal controlled reference channel of wideband analog FM recording systems without having to wait for the system to warm-up and stabilize.

The modulation ASIC was also designed to generate other types of modulation under computer control (phase modulation, amplitude modulation, PSK, FSK, QAM, etc.). With the success of the development of the DFM for digital FM multiplexing, the potential for fast growth of future products is exciting. In the near future it will be possible to produce a computer controlled, mixed modulation system using just one standard instrument.

## ACKNOWLEDGMENTS

Carl Smith and Charles Reisel were key contributors to the overall conceptual design work described in this paper. The author appreciates the efforts of these individuals as well as the other members of the project design team.

## REFERENCES

1. DeFatta, David, et al, Digital Signal Processing, John Wiley & Sons, New York, 1988, pp. 60-61.
2. Cooper, Hamil, "Why Complicate Frequency Synthesis?", Electronic Design, Vol 15, July 19, 1974, p. 80-84.