

# ARCHI-PCM

Handheld Portable Complete Standalone PCM Processing System

Single or Dual Channel



The industry's first fully handheld, self-contained, portable PCM processing system which includes bit sync, frame sync, PCM decom, IRIG Time Code Reader, PCM simulator, and full feature PCM BERT. The ARCHI contains an integrated graphical display, touchscreen, Ethernet setup, and UDP Ethernet output of frame and parameter data to Ulyssix ALTAIR software or user custom software.

Optional capabilities include Chapter 10 storage and Ethernet interface, and TMoIP data.



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# ARCHI Product Features

**The ARCHI is a standalone 10" x 8.5" x 3" aluminum enclosure that houses the Ulyssix 4th generation Tarsus4-PCIe card for portable and remote PCM Processing powered by USB-C power delivery (PD) using an external USB-C PD 67W AC/DC adapter, by using a laptop computer USB-C PD or Thunderbolt interface.**

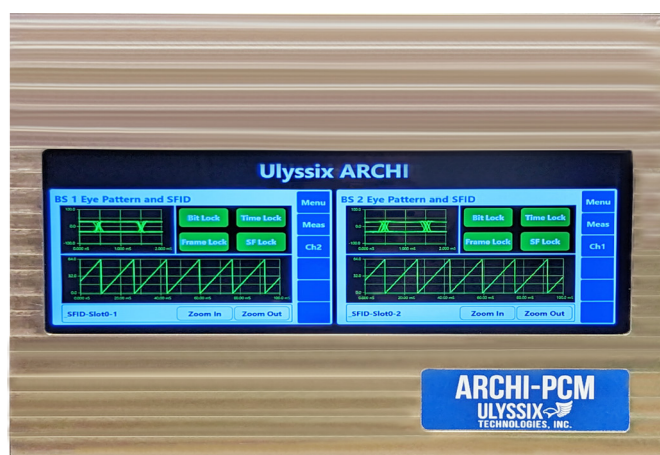
## PCM Processor to Ethernet Packets

The new ARCHI PCM Processing system allows the telemetry user to travel without a large computer housing and a standalone 3U PCIe card. The ARCHI system is the size of a textbook and connects to a laptop or any remote computer via Ethernet and is powered either by the laptop's USB-C PD or a wall adapter that is supplied with the unit. The ARCHI has a graphic display/touchscreen for setup and monitoring as well as can be setup and monitored via any computer (laptop or rackmount) using the Ulyssix ALTAIR software. All inputs/outputs to the ARCHI are via mounted BNC connectors on the side of the handheld unit. The ARCHI can interface directly to user developed CH10 or TMoIP software or other commercial software suites with these IP input capability.

The PCM decommutated data from the ARCHI will be available on the user's laptop running the Ulyssix ALTAIR software (included with the ARCHI system) as well as to a 9.3" x 3.7", 1600 x 600 HDMI interface with touchscreen capability. Data will be displayed, analyzed, stored, and/or Ethernet transported in either PCM UDP transport, Chapter 10 PCM data packets, Chapter 7 integrated data packets, or TMoIP packets to other users.

The fully integrated ARCHI housing contains the Ulyssix Tarsus4-PCIe 4th generation PCM Processing card, with an embedded INTEL core processing single board computer, 1 TB SSHD, with a PCIe slot for communication to the Tarsus4-PCIe and independent USB-C PD power distribution. The Ulyssix ALTAIR software is embedded in the ARCHI.

A future upgrade to the ARCHI portable system will be the integration of the Bald Eagle4-RF dual receiver module to create a truly portable RF to Ethernet solution.



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# ARCHI-PCM Specifications

## Bit Synchronizer Input Specifications

|                           |                                                                                                                           |
|---------------------------|---------------------------------------------------------------------------------------------------------------------------|
| Input Data Rate           | Bit Sync programmable input tunable rates from 1 bps to 40 Mbps for NRZ-L/M/S, RNRZ-L and 1 bps to 20 Mbps for Bi-Φ L/M/S |
| Input Source              | 2 independent inputs (1 single ended BNC, 1 differential Twinax)                                                          |
| Input Impedance           | Hi-Z/75Ω/50Ω, single ended input, software selectable                                                                     |
| Maximum Safe Input        | ± 35 VDC                                                                                                                  |
| Input Signal Level        | 30 mVp-p to 5 Vp-p                                                                                                        |
| DC Input Level            | +/- 5 VDC                                                                                                                 |
| Input PCM Codetypes Modes | NRZ-L/M/S, RNRZ-L, RZ, Bi-Φ L/M/S, program selectable (consult factory for other codetypes)                               |
| Derandomizer Input        | RNRZ-11/15, forward/reverse, program selectable                                                                           |
| Input Polarity            | Normal, inverted or auto selectable using frame sync correlator                                                           |

## Bit Synchronizer Data Specifications

|                        |                                                                                                                                                                                       |
|------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Loop Bandwidth         | 0.01% to 3.0%, to the programmed bit rate                                                                                                                                             |
| Capture Range          | +/-3 times of the programmed loop bandwidth                                                                                                                                           |
| Data Tracking Range    | +/-5 times of the programmed loop bandwidth                                                                                                                                           |
| Sync Acquisition       | less than 200 bits, typically 100 bits max                                                                                                                                            |
| Bit Error Probability  | Less than 1 dB to theoretical bit sync BER performance for bit rates up to 25 Mbps, less than 2 dB to theoretical from 25 Mbps to 33 Mbps, less than 2.7 dB to theoretical to 40 Mbps |
| PCM Encoder Output     | TTL and RS-422 Level driven                                                                                                                                                           |
| PCM Encoder Code Types | NRZ-L/M/S, RNRZ-L, RZ, Bi-Φ L/M/S or RNRZ 11/15, program selectable                                                                                                                   |
| Clock Output           | 0°, 90°, 180°, 270°                                                                                                                                                                   |

## Frame Sync/Decommutator Specifications

|                                    |                                                                                                                   |
|------------------------------------|-------------------------------------------------------------------------------------------------------------------|
| Input Data Rate                    | Up to 50 Mbps                                                                                                     |
| Input Signals                      | TTL Level single ended, RS-422 differential or direct from Bit Sync section of the PCM Processor, NRZ-L and clock |
| Word Lengths                       | 3 to 64 bits variable from channel to channel                                                                     |
| Minor Frame Length                 | 3 to 65,536 bits                                                                                                  |
| Major Frame Length                 | 1 to 1024 minor frames per major frame                                                                            |
| PCM bit word order                 | MSB or LSB, word by word basis, program selectable                                                                |
| Frame Sync Pattern                 | 16 to 64 bits                                                                                                     |
| Frame Sync Location                | Leading the minor frame                                                                                           |
| Frame Sync Strategy                | Search-Check-Lock, programmable counts per step                                                                   |
| Subframe Sync                      | FCC or SFID                                                                                                       |
| Sync Error Tolerance               | 0 to 8 bits, program selectable                                                                                   |
| Bit Slip Window                    | 0 to 9999 bits, program selectable                                                                                |
| Data Polarity                      | Normal or inverted on a channel by channel basis                                                                  |
| Asynchronously Embedded Formats    | Supports up to 8 asynchronous embedded formats with 5 levels deep based on computer CPU capability                |
| Bit Concatenation/Fragmented-Words | Software decommutator can combine individual bits from separate PCM words                                         |

## PCM Simulator Specifications

|                      |                                                                                                             |
|----------------------|-------------------------------------------------------------------------------------------------------------|
| Output Data Rate     | 1 bps to 40 Mbps for NRZ-x, RNRZ-L, or 20 Mbps for all others                                               |
| Output PCM Codetypes | NRZ-L/M/S, RNRZ-L 11/15, RZ, Bi-Φ L/M/S, RNRZ 11/15/, forward/reverse, program selectable                   |
| Output Signal Levels | Data and Clock, TTL, and RS422 level driven                                                                 |
| Data Words           | Fixed or math functions (sine wave, triangle, square wave, sawtooth, counter) with programmable sample rate |

## Bit Error Rate Tester (BERT) Specification

|                |                                                                                             |
|----------------|---------------------------------------------------------------------------------------------|
| Input Data     | User selectable including PN11, PN15, simulator data or user created .bin file              |
| Bit Rate       | User selectable 1 bps to 40 Mbps                                                            |
| Testing Method | Each individual bit error checking with user configurable interval and cumulative readings. |

## DAC Output Specification

|                    |                                                                             |
|--------------------|-----------------------------------------------------------------------------|
| Number of Channels | 2                                                                           |
| Output Level       | 1 Vpp to 5 Vpp, selectable in 0.1 Vpp steps, ± 2.5V offset in 0.1 VDC steps |

## Time Code Reader Specifications

|                |                                                                      |
|----------------|----------------------------------------------------------------------|
| IRIG Codetypes | AM Modulated - IRIG A, B, G & NASA-36<br>DC Input - IRIG-B DC LS/TTL |
|----------------|----------------------------------------------------------------------|

## ARCHI Data Storage

|                |                                                                                               |
|----------------|-----------------------------------------------------------------------------------------------|
| Storage Amount | 1 TB using on board SSHD                                                                      |
| Data Retrieval | Through supplied software suite or user generated software using Ulyssix data software driver |

## ARCHI Diagnostics

|                     |                                                                                      |
|---------------------|--------------------------------------------------------------------------------------|
| Version Control     | All current software, firmware, and driver version numbers stored for easy retrieval |
| Latest Setup        | Current card setup configuration is stored for verification of proper setup          |
| Diagnostic Download | Direct download to file for transfer to Ulyssix for evaluation and recommendations   |

## Physical Specifications

|                       |                                                                                                                                               |
|-----------------------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| Mechanical Dimensions | 10" x 8.5" x 3" Mechanical housing with internal Tarsus4-PCIe card                                                                            |
| Interface Connectors  | MDM-51 connector to individual BNC breakout cables (other configurations, consult factory)                                                    |
| Manufacturing         | The design utilizes Surface Mount Technology (SMT), manufactured with robotic assembly techniques to IPC-610B Class 2 manufacturing standards |
| Temperature Range     | Operating: 0°C to 70°C<br>Storage: -20°C to 85°C                                                                                              |
| Power Consumption:    | Less than 35 Watts total, for all supplies<br>+3.3V 3.5 Amps<br>+12V 0.8 Amps                                                                 |

## Ordering Options

|                  |                                                                                                                                                                                                                                                                                                  |
|------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ARCHI-PCM-01     | Portable Single Channel PCM Processing System powered by USB-C PD with Ethernet Interface                                                                                                                                                                                                        |
| ARCHI-PCM-02     | Portable Dual Channel PCM Processing System powered by USB-C PD with Ethernet Interface                                                                                                                                                                                                          |
| ULX-OPT-UART     | Upgrade to add 4 UART RS-232 channel outputs                                                                                                                                                                                                                                                     |
| ULX-OPT-CH7/CH10 | Receive Chapter 7 Ethernet packets and process the Chapter 10 PCM packets within the Chapter 7 transmission. This option also allows the user to record the IRIG Chapter 10 format and playback through the archive simulator plus UDP Ethernet transmission and reception in Chapter 10 packets |
| ULX-OPT-CH10     | Chapter 10 recording and reproducer for both Chapter 10 disk files and UDP-CH10-Ethernet packets                                                                                                                                                                                                 |

**Features are subject to change without notice.**

**Revised: August 14, 2025**