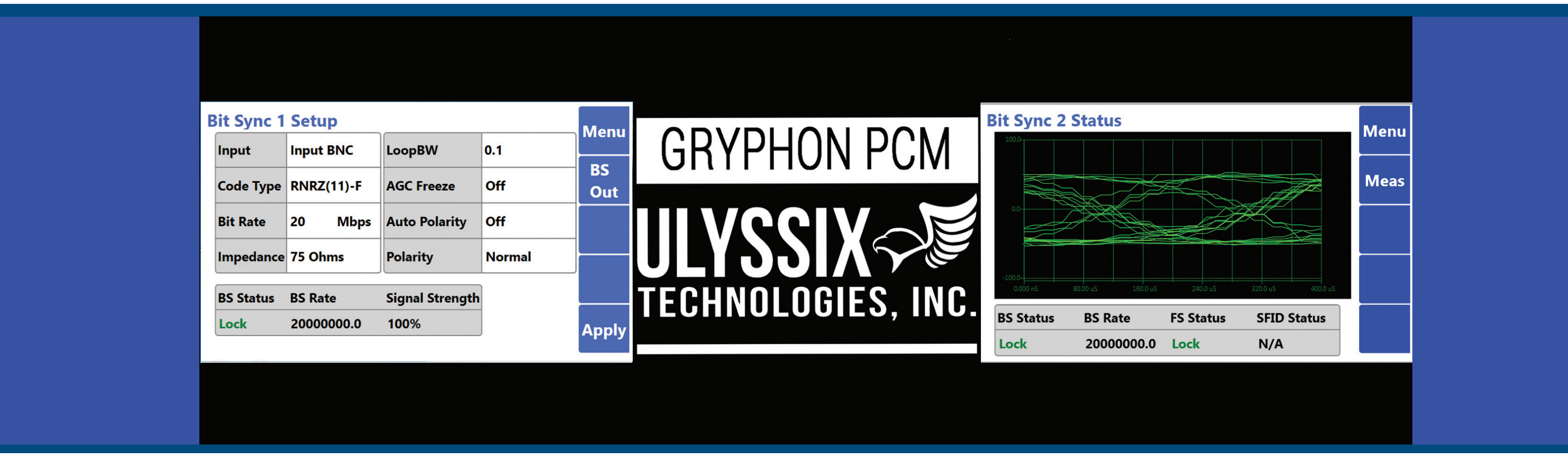
Gryphon PCM-DC

Rackmount 40 Mbps Dual PCM Processing System



Dual Bit Sync/Dual Frame Sync/Frame Archiver/IRIG Time Code Reader/PCM Baseband Simulator with Optional Dual PCM Decommutator Chapter 10 Storage/Ethernet Transmission/BERT/Baseband Functionality

External UL/CEC Listed AC/DC Adapter Included

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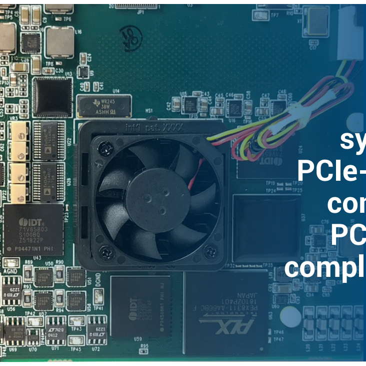
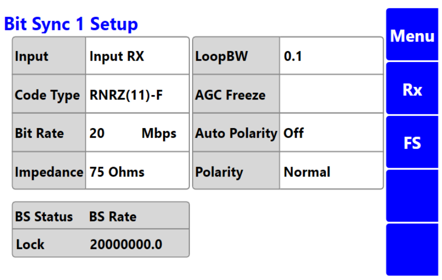
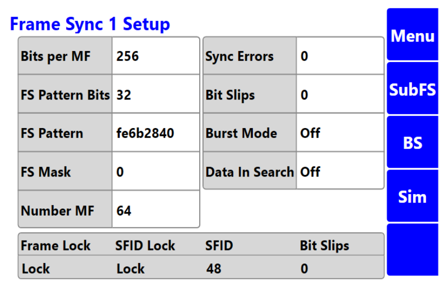


Gryphon PCM-DC

Ulyssix's Gryphon PCM-DC 2U rackmount is complete baseband telemetry system. The Gryphon PCM-DC system uses the combined advanced 3rd generation Tarsus3-PCIe-02 with an embedded processor. The full functionality of the Ulyssix solution gives the use complete baseband data acquisition with data processing in this single solution. The Gryphon PCM-DC is set up and controlled by dual high-resolution color HDMI touchscreen displays for complete flexibility using the front panel touchscreen interface. The Gryphon PCM-DC solution is powered by the latest INTEL/Altera FPGA technology with user upgradable DSP firmware algorithms.

Gryphon PCM-DC 2U Dual Bit/ Frame Sync System





Bit Synchronizer

Designed using all DSP filter algorithms in FPGA technology for maximum performance capability

Accepts all IRIG 106 PCM code types

Bit Sync programmable input rates from 1 bps to 40 Mbps

Less than 1 dB to theoretical bit sync BER performance

Integrated graphic eye pattern display for complete lock indication

Frame Synchronizer

Supports PCM streams from 1 bps up to 50 Mbps

Supports up to 1024 minor frames per major frame and 16 M bits per minor frame

Frame Sync Archive capability

Advanced algorithm to allow for varying frame sizes

Input either from bit sync or external clock and data

Storage & Diagnostics

Diagnostic feature used to aid Ulyssix in trouble-shooting FPGA firmware internal control register configuration from user setup configuration

Retrieval popup form in GRYPHON software suites outputs diagnostic file for transfer to Ulyssix for quick system analysis for card configuration errors, setup errors, or actual hardware failures

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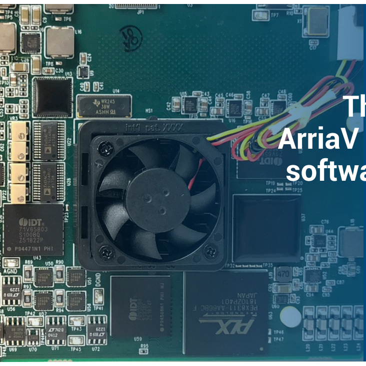


Gryphon PCM-DC

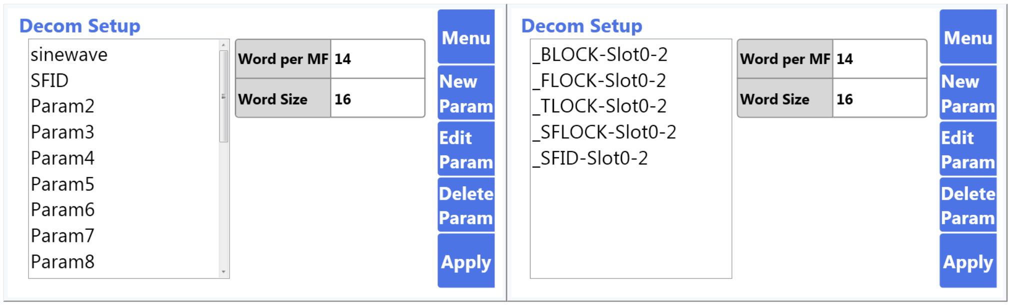
The Gryphon PCM-DC Tarsus3 PCM processor board is powered by the latest INTEL/ALTERA ArriaV GZ and Cyclone III FPGA's. The firmware is user reconfigurable using the Gryphon PCM-DC software suite with user upgradable capability when under maintenance contract. Using optional Chapter 10 Ethernet or UDP Parameter/Broadcast licensed features, the Gryphon PCM-DC system can be used for remote monitoring of time tagged frame lock PCM data.

Gryphon PCM-DC Features:

Features Included:
Dual Multi-Mode Receivers
Dual PCM Baseband
IRIG Time Code Reader
PCM Simulator Setup

Optional Features:

RF Modulating Generator
IRIG CH10 Recorder/Playback
UDP Frame and Parameter Broadcasting
Internal BERT Operation
Dual Decommutator
Viterbi Decoder



IRIG Time Code Reader

IRIG Time interpolated to 1 usec resolution

Supports DC Level IRIG-B and AM Modulated IRIG A, B, G & NASA-36

Used for both IRIG time display and/or minor frame time tag header information

PCM Simulator

Programmable PCM streams from 1 bps up to 40 Mbps

Ulyssix .tad frame sync file and Chapter 10 Archive playback capability

Fixed major frame simulator utilizing defined waveform & tabular data to output

Convolutional Encoder output capable for Viterbi Simulator

Selectable output code type

TTL and RS422 output capability

Optional Decommutator

Supports all IRIG Class II decommutator features with variable word length from 3 - 64 bits, format switching, parameter concatenation, and asynchronous embedded formats

High speed data transfer of user word selected channels to the PCI bus for disk storage and playback

Two on card DACs for word analog output

Full parameter math processing

Available with Ulyssix ALTAIR Software Suite for full setup of format frame, word selection, channel display capability and optional client/server capability

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Gryphon PCM-DC
PCM Processor Specifications*

Bit Synchronizer Input Specifications

Input Data Rate	Bit Sync programmable input tunable rates from 1 bps to 40 Mbps for NRZ-L/M/S, RNRZ-L, and 1 bps to 20 Mbps for Bi-Φ L/M/S
Input Source	2 independent inputs (1 single ended BNC, 1 differential Twinax)
Input Impedance	Hi-Z/75Ω/50Ω, single ended input, software selectable, BNC input, 120 ohms Differential
Maximum Safe Input	± 35 VDC
Input Signal Level	30 mVp-p to 5 Vp-p
DC Input Level	+/- 5 VDC
Input PCM Codetypes Modes	NRZ-L/M/S, RNRZ-L, RZ, Bi-Φ L/M/S, program selectable (consult factory for other codetypes)
Derandomizer Input	RNRZ-11/15, forward/reverse, program selectable
Input Polarity	Normal, inverted, or auto selectable using frame sync correlator

Bit Synchronizer Data Specifications

Loop Bandwidth	0.01% to 3.0%, to the programmed bit rate
Capture Range	+/-3 times of the programmed loop bandwidth
Data Tracking Range	+/-5 times of the programmed loop bandwidth
Sync Acquisition	Less than 200 bits, typically 100 bits max
Bit Error Probability	Less than 1 dB to theoretical bit sync BER performance for bit rates up to 25 Mbps, less than 2 dB to theoretical from 25 Mbps to 40 Mbps
Bity Sync Output	TTL and RS422 Level driven
Bit Sync Code Types	NRZ-L/M/S, RNRZ-L, RZ, Bi-Φ L/M/S, or RNRZ 11/15, program selectable
Clock Output	0°, 90°, 180°, 270°

Frame Sync/Optional Decommutator Specifications

Input Data Rate	Up to 50 Mbps
Input Signals	TTL Level single ended, RS-422 differential or direct from Bit Sync section of the PCM Processor, NRZ-L and clock
Word Lengths	3 to 64 bits variable from channel to channel
Minor Frame Length	3 to 16,777,216 bits
Major Frame Length	1 to 1024 minor frames per major frame
PCM bit word order	MSB or LSB, word by word basis, program selectable
Frame Sync Pattern	16 to 64 bits
Frame Sync Location	Leading the minor frame
Frame Sync Strategy	Search-Check-Lock, programmable counts per step
Subframe Sync	FCC or SFID
Sync Error Tolerance	0 to 8 bits, program selectable
Bit Slip Window	0 to 9999 bits, program selectable
Data Polarity	Normal or inverted on a channel by channel basis
Asynchronously Embedded Formats	Supports up 8 asynchronous embedded formats based on computer CPU capability
Bit Concatenation/Fragmented Words	Software decommutator can combine individual bits from separate PCM words

DAC Output Specifications

Number of Channels	2
Output Level	1 Vpp to 5 Vpp, selectable in 0.1 Vpp steps, ± 2.5V offset in 0.1 VDC steps

PCM Simulator Specifications

Output Data Rate	1 bps to 40 Mbps for NRZ-x, RNRZ-L, or 20 Mbps for all others
Output PCM Codetypes	NRZ-L/M/S, RNRZ-L 11/15, RZ, Bi-Φ L/M/S, RNRZ 11/15/, forward/reverse, program selectable
Output Signal Levels	Data and Clock, TTL, and RS422 level driven
Word Lengths	3 to 64 bits, variable length
Frame Length	Same as decommutator specs
Data Words	Fixed or math functions (sine wave, triangle, square wave, sawtooth, counter) with programmable sample rate

Time Code Reader Specifications

IRIG Codetypes	DC Level IRIG-B and AM Modulated IRIG A, B, G, & NASA-36

Gryphon PCM-DC Diagnostics

Version Control	All current software, firmware and driver version numbers stored for easy retrieval
Latest Setup	Current card setup configuration is stored for verification of proper setup
Diagnostic Download	Direct download to file for transfer to Ulyssix for evaluation and recommendations

Physical Specifications

Dimensions	2U 19" rackmount chassis with 100V-240V AC input capability
Interface Connectors	Baseband PCM inputs and outputs through single ended 75 ohm BNC rackmount connectors & Differential Twinax
Manufacturing	The design utilizes Surface Mount Technology (SMT), manufactured with robotic assembly techniques to IPC-610B Class 2 manufacturing standards
Temperature Range	Operating: 0°C to 50°C Storage: -20°C to 60°C
Power Consumption	250 Watts / 300 watts peak
DC Input Voltage	6-30 Volts, using standard Molex 2x3 469930619 connector
AC/DC External Power Adapter (included with Gryphon PCM-DC)	24 VDC, 250 Watts, 100~240 VAC Nominal Ul/cUL 62368-1, 60950-1; CE: IEC 62368-1, 60950-1

Ordering Options

Gryphon PCM-DC	2U rackmount Dual, Dual PCM Processing capability, IRIG Time Code Reader, PCM Simulation and BERT Tester Option for Bit Error Tester of RF, and PCM Data Stream
ULX-OPT-CH10	Chapter 10 recording and reproducer for both Chapter 10 disk files and UDP-CH10-Ethernet packets
ULX-OPT-IRIGTIMEOUT	Optional IRIG Time output from .tad archive file playback
ULX-OPT-LQTESTER	BERT Tester Option for Time Latency Measurements and Bit Error Tester of PCM Data Stream
ULX-OPT-RTSIM	Optional real-time simulator parameter variability. Used to change parameters while running simulator
ULX-OPT-UDP PARAM/FRAME BROADCAST	UDP Frame and/or decom parameter multicast or unicast broadcast for external ALTAIR software networking or external data transfer
ULX-OPT-Viterbi	Viterbi decoding solution

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***Specifications are subject to change without notice.**
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