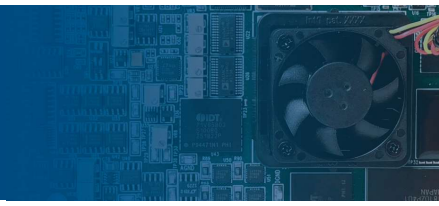
Gryphon PCM
PCM Processor Specifications*



Bit Synchronizer Input Specifications

Input Data Rate	Bit Sync programmable input tunable rates from 1 bps to 40 Mbps for NRZ-L/M/S, RNRZ-L, and 1 bps to 20 Mbps for Bi-Φ L/M/S
Input Source	2 independent inputs (1 single ended BNC, 1 differential Twinax)
Input Impedance	Hi-Z/75Ω/500Ω, single ended input, software selectable, BNC input, 120 ohms Differential
Maximum Safe Input	± 35 VDC
Input Signal Level	30 mVp-p to 5 Vp-p
DC Input Level	+/- 5 VDC
Input PCM Codetypes Modes	NRZ-L/M/S, RNRZ-L, RZ, Bi-Φ L/M/S, program selectable (consult factory for other codetypes)
Derandomizer Input	RNRZ-11/15, forward/reverse, program selectable
Input Polarity	Normal, inverted, or auto selectable using frame sync correlator

Bit Synchronizer Data Specifications

Loop Bandwidth	0.01% to 3.0%, to the programmed bit rate
Capture Range	+/-3 times of the programmed loop bandwidth
Data Tracking Range	+/-5 times of the programmed loop bandwidth
Sync Acquisition	Less than 200 bits, typically 100 bits max
Bit Error Probability	Less than 1 dB to theoretical bit sync BER per-formance for bit rates up to 25 Mbps, less than 2 dB to theoretical from 25 Mbps to 40 Mbps
Bity Sync Output	TTL and RS422 Level driven
Bit Sync Code Types	NRZ-L/M/S, RNRZ-L, RZ, Bi-Φ L/M/S, or RNRZ 11/15, program selectable
Clock Output	0°, 90°, 180°, 270°

Frame Sync/Optional Decommutator Specifications

Input Data Rate	Up to 50 Mbps
Input Signals	TTL Level single ended, RS-422 differential or direct from Bit Sync section of the PCM Processor, NRZ-L and clock
Word Lengths	3 to 64 bits variable from channel to channel
Minor Frame Length	3 to 16,777,216 bits
Major Frame Length	1 to 1024 minor frames per major frame
PCM bit word order	MSB or LSB, word by word basis, program selectable
Frame Sync Pattern	16 to 64 bits
Frame Sync Location	Leading the minor frame
Frame Sync Strategy	Search-Check-Lock, programmable counts per step
Subframe Sync	FCC or SFID
Sync Error Tolerance	0 to 8 bits, program selectable
Bit Slip Window	0 to 9999 bits, program selectable
Data Polarity	Normal or inverted on a channel by channel basis
Asynchronously Embedded Formats	Supports up 8 asynchronous embedded formats based on computer CPU capability
Bit Concatenation/Fragmented Words	Software decommutator can combine individual bits from separate PCM words

DAC Output Specifications

Number of Channels	2
Output Level	1 Vpp to 5 Vpp, selectable in 0.1 Vpp steps, ± 2.5V offset in 0.1 VDC steps

PCM Simulator Specifications

Output Data Rate	1 bps to 40 Mbps for NRZ-x, RNRZ-L, or 20 Mbps for all others
Output PCM Codetypes	NRZ-L/M/S, RNRZ-L 11/15, RZ, Bi-Φ L/M/S, RNRZ 11/15/, forward/reverse, program selectable
Output Signal Levels	Data and Clock, TTL, and RS422 level driven
Word Lengths	3 to 64 bits, variable length
Frame Length	Same as decommutator specs
Data Words	Fixed or math functions (sine wave, triangle, square wave, sawtooth, counter) with programmable sample rate

Time Code Reader Specifications

IRIG Codetypes	DC Level IRIG-B and AM Modulated IRIG A, B, G, & NASA-36

Gryphon PCM Diagnostics

Version Control	All current software, firmware and driver version numbers stored for easy retrieval
Latest Setup	Current card setup configuration is stored for verification of proper setup
Diagnostic Download	Direct download to file for transfer to Ulyssix for evaluation and recommendations

Physical Specifications

Dimensions	2U 19" rackmount chassis with 100V-240V AC input capability
Interface Connectors	Baseband PCM inputs and outputs through single ended 75 ohm BNC rackmount connectors & Differential Twinax
Manufacturing	The design utilizes Surface Mount Technology (SMT), manufactured with robotic assembly techniques to IPC-610B Class 2 manufacturing standards
Temperature Range	Operating: 0°C to 50°C Storage: -20°C to 60°C
Power Consumption	Less than 300 Watts

Ordering Options

Gryphon-PCM-Dual or -Quad	2U rackmount PCM Processing capability, IRIG Time Code Reader, PCM Simulation and BERT Tester Option for Bit Error Tester of RF and PCM Data Stream
ULX-OPT-CH10	Chapter 10 recording and reproducer for both Chapter 10 disk files and UDP-CH10-Ethernet packets
ULX-OPT Dual Decom	Optional Word Selector with Graphic Displays for Individual Decom Parameter Procession
ULX-OPT-IRIGTIMEOUT	Optional IRIG Time output from .tad archive file playback
ULX-OPT-LQTESTER	BERT Tester Option for Time Latency Measurements and Bit Error Tester of PCM Data Stream
ULX-OPT-RTSIM	Optional real-time simulator parameter variability. Used to change parameters while running simulator
ULX-OPT-TMoIP	ALTAIR Software Upgrade for telemetry over IP
ULX-OPT-UDP PARAM/FRAME BROADCAST	UDP Frame and/or decom parameter multicast or unicast broadcast for external ALTAIR software networking or external data transfer
ULX-OPT-Viterbi	Viterbi decoding solution

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Specifications are subject to change without notice.
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