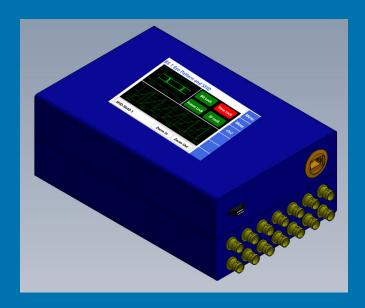
ARCHI

Handheld Portable Standalone Complete PCM Processing System





The industry's first fully handheld, self-contained, portable PCM processing system with integrated graphical display, touchscreen, Ethernet setup, and Ethernet output of Chapter 10, TMoIP data, or .tad frame data.



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ARCHI Product Features

The ARCHI is a standalone 9" x 6" x 3" enclosure that houses the Tarsus4-PCIe card for remote PCM Processing powered by USB-C power delivery (PD) using an external USB-C PD 67W AC/DC adapter or by using a laptop computer USB-C PD or Thunderbolt interface.

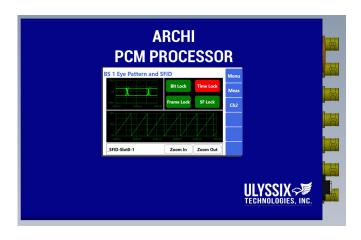
PCM Processor to Ethernet Packets

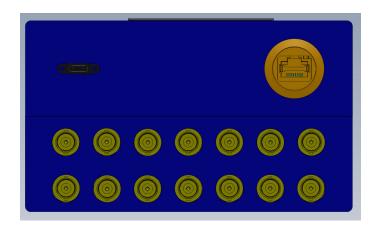
The new ARCHI system allows the telemetry user to travel without a large computer housing and a standalone 3U PCIe card. The ARCHI system is the size of a textbook and connects to a laptop via Ethernet and is powered either by the laptop's USB-C PD or a wall adapter that is supplied with the unit. The ARCHI has a graphic display/touchscreen for setup and monitoring as well as can be setup and monitored via any computer (laptop or rackmount) using the Ulyssix ALTAIR software. All inputs/outputs to the ARCHI are via mounted BNC connectors on the side of the handheld unit. The ARCHI can interface directly to user developed CH10 or TMoIP software or other commercial software suites with these IP input capability.

The PCM decommuated data from the ARCHI will be available on the user's laptop running the Ulyssix ALTAIR software (included with the ARCHI system) as well as to a 4.3", 800x480 HDMI interface with touchscreen capability. Data will be displayed, analyzed, stored, and/or Ethernet transported in either PCM UDP transport, Chapter 10 PCM data packets, Chapter 7 integrated data packets, or TMoIP packets to other users.

The fully integrated ARCHI housing contains the Ulyssix Tarsus4-PCIe 4th generation, with an embedded small processor card with a PCIe slot for communication to the Tarsus4-PCIe and independent USB-C PD power distribution. The Ulyssix ALTAIR software is embedded in the ARCHI.

A future upgrade to the ARCHI portable system will be the integration of the Bald Eagle4-RF dual receiver module to create a truly portable RF to Ethernet solution.





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ARCHI Specifications

Data Words

Bit Synchronizer Input Specifications		DAC Output Specification	
Input Data Rate	Bit Sync programmable input tunable rates from	Number of Channels	4
•	1 bps to 40 Mbps for NRZ-L/M/S, RNRZ-L and 1 bps to 20 Mbps for Bi-Ф L/M/S	Output Level	1 Vpp to 5 Vpp, selectable in 0.1 Vpp steps, \pm 2.5 offset in 0.1 VDC steps
Input Source	2 independent inputs (1 single ended BNC, 1 differential Twinax)	Time Code Reader Specifications	
Input Impedance	Hi-Z/75Ω/50Ω, single ended input, software selectable	IRIG Codetypes	AM Modulated - IRIG A, B, G & NASA-36 DC Input - IRIG-B DC LS/TTL
Maximum Safe Input	± 35 VDC	On Card Data Storage - 1	l Optional
Input Signal Level	30 mVp-p to 5 Vp-p	Storage Amount	Up to 32 GB archived data stored in 32-bit packet
DC Input Level	+/- 5 VDC	Data Retrieval	format
Input PCM Codetypes Modes	NRZ-L/M/S, RNRZ-L, RZ, Bi-Φ L/M/S, program selectable (consult factory for other codetypes)		Through supplied software suite or user generate software using Ulyssix data software driver
Derandomizer Input	RNRZ-11/15, forward/reverse, program selectable	ARCHI Diagnostics Version Control	All current software, firmware, and driver version
Input Polarity	Normal, inverted or auto selectable using frame sync correlator	Latest Setup	numbers stored for easy retrieval Current card setup configuration is stored for
Bit Synchronizer Data S	,	·	verification of proper setup
	•	Diagnostic Download	Direct download to file for transfer to Ulyssix for evaluation and recommendations
Loop Bandwidth Capture Range	0.01% to 3.0%, to the programmed bit rate +/-3 times of the programmed loop bandwidth	Physical Specifications	evaluation and recommendations
Data Tracking Range	+/-5 times of the programmed loop bandwidth	,	O"vC"vQ" Machanical barrier with internal
Sync Acquisition	less than 200 bits, typically 100 bits max	Mechanical Dimensions	9"x6"x3" Mechanical housing with internal Tarsus4-PCle card
Bit Error Probability	Less than 1 dB to theoretical bit sync BER performance for bit rates up to 25 Mbps, less	Interface Connectors	MDM-51 connector to individual BNC breakout cables (other configurations, consult factory)
DOME - LOCAL	than 2 dB to theoretical from 25 Mbps to 33 Mbps, less than 2.7 dB to theoretical to 40 Mbps	Manufacturing	The design utilizes Surface Mount Technology (SMT), manufactured with robotic assembly techniques to IPC-610B Class 2 manufacturing
PCM Encoder Output	TTL and RS-422 Level driven		standards
PCM Encoder Code Types	NRZ-L/M/S, RNRZ-L, RZ, Bi-Ф L/M/S or RNRZ 11/15, program selectable 0°, 90°, 180°, 270°	Temperature Range	Operating: 0°C to 70°C Storage: -20°C to 85°C
Clock Output		Power Consumption:	Less than 25 Watts total, for all supplies
Frame Sync/Decommu			+3.3V 3.5 Amps +12V 0.8 Amps
Input Data Rate	Up to 50 Mbps	Ordaring Ontions	112V 0.0 Amps
Input Signals	TTL Level single ended, RS-422 differential or direct from Bit Sync section of the PCM Processor, NRZ-L and clock	Ordering Options ARCHI-PCM	Portable PCM Processing System powered by USB-C PD with Ethernet Interface
Word Lengths	3 to 64 bits variable from channel to channel		COD OT D With Ethernet interface
Minor Frame Length	3 to 16,777,216 bits	ULX-OPT-UART	Upgrade to add 4 UART RS-232 channel outputs
Major Frame Length	1 to 1024 minor frames per major frame	ULX-OPT-CH7/CH10	Receive Chapter 7 Ethernet packets and process the Chapter 10 PCM packets within the Chapter 7 transmission. This option also allows the user to record the IRIG Chapter 10 format and playback through the archive simulator plus UDP Ethernet
PCM bit word order	MSB or LSB, word by word basis, program selectable		
Frame Sync Pattern	16 to 64 bits		
Frame Sync Location	Leading the minor frame		transmission and reception in Chapter 10 packet
Frame Sync Strategy	Search-Check-Lock, programmable counts per step	ULX-OPT-CH10	Chapter 10 recording and reproducer for both Chapter 10 disk files and UDP-CH10-Ethernet
Subframe Sync	FCC or SFID	ULX-OPT-LQTESTER	packets PERT Tester Ontion for Time Latency Measure-
Sync Error Tolerance	0 to 8 bits, program selectable	OLX-OF I-LQTESTEN	BERT Tester Option for Time Latency Measure- ments and Bit Error Tester of PCM Data Stream
Bit Slip Window Data Polarity	0 to 9999 bits, program selectable Normal or inverted on a channel by channel basis	ULX-OPT-UDP PARAM/FRAME BROADCAST	UDP Frame and/or decom parameter mulitcast or unicast broadcast for external Altair software
Asynchronously Embedded Formats	Supports up to 8 asynchronous embedded formats with 5 levels deep based on computer CPU capability		networking or external data transfer
Bit Concatenation/Fragmented- Words	Software decommutator can combine individual bits from separate PCM words		
PCM Simulator Specific	cations		
Output Data Rate	1 bps to 40 Mbps for NRZ-x, RNRZ-L, or 20 Mbps for all others		
Output PCM Codetypes	NRZ-L/M/S, RNRZ-L 11/15, RZ, Bi-Φ L/M/S, RNRZ 11/15/, forward/reverse, program selectable		
Output Signal Levels	Data and Clock, TTL, and RS422 level driven		
Nata Words	Fixed or math functions (sine wave triangle	Features	are subject to change without notice.

Fixed or math functions (sine wave, triangle, square wave, sawtooth, counter) with

programmable sample rate

Features are subject to change without notice. Revised: February 7, 2025